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ON THE USE OF PHYSICS BASED MODELS IN HARDWARE DESIGN AND CONTROL

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ABSTRACT

A discussion on the utility of physics-based compact thermal models to guide the design, integration, operation and control of thermally sensitive vehicle components is presented. Effective component selection requires honest and accurate representation of the key performance attributes expressed by physics-based models. Parallel developments and lessons learned from the Electronics Industry on component packaging and characterization is discussed. An example application of a physics-based model driven design is presented for an Electrical Energy Dissipater design used on typical hybrid vehicles. Low fidelity models are used early in the design to support system requirements decomposition into discreet design attributes. High fidelity thermal and electromagnetic models are used to explore the design space and to optimize performance metrics. Accurate and robust reduced order thermal models are used for the continuous prognostic, diagnostic monitoring and control of the device.

INTRODUCTION

The design process for components and subsystems intended for use in modern day Military Ground Vehicles encounters broad challenges that encompass extremes in operating environments, severe weight and space constraints and integration challenges brought about by the synthesis of disparate and complex components and subsystems into an objective system that seeks to maximize vehicle performance. The availability of physics-based component models provides the necessary foundation for understanding component capabilities, anticipating performance limitations, and enabling the development of vehicle thermal, power and control architectures.

Hardware integration onto a vehicle platform quite often exposes equipment to a thermal environment that may differ from the underlying assumptions used for the design and development of that hardware. This may be the result of any number of factors including updates in the requirements and specifications, changes in the anticipated mission profile, or even integration onto a different vehicle platform other than the one that the equipment was originally developed for.

In a Modeling and Simulation centric environment the process of component and subsystem hardware design and development is supported by physics-based models that provide the appropriate level of fidelity at each stage of the product development process. For this approach to be successful it becomes necessary to develop and adopt modeling standards that provide a common platform for component integration and control. This can be accomplished by the development of compact or low fidelity models that are capable of accurately describing the response of these systems as a function of their surrounding environment and usage. This approach will facilitate the protection of the intellectual property (IP) of equipment suppliers since it does not necessitate the disclosure of the underlying design details in order to provide a simulation framework for assessing, evaluating, and resolving integration related issues quickly, at lower cost, and with a reasonable level of fidelity and confidence.

Hardware Characterization in Electronics Industry

The electronics and semiconductor industries face a similar challenge in dealing with integration of components, boards, and IC devices onto systems. In the early 1990's some European industries begun to realize that accurate temperature predictions of critical electronics parts at the package, board, and system level was hampered by the lack of reliable standardized input data that characterize the thermal behavior of these parts. This was the start of a series of European funded projects dealing with the development and experimental verification of thermal models for numerous standard components. An excellent summary of the history, background, philosophy and underlying methodology behind these developments can be found in Lasance [1]. The first project, coined the DELPHI project, was driven exclusively by end users. The DELPHI project dealt with the definition of the development methodology needed for the creation of Compact Thermal Models (CTMs). These models typically provide a representation of the interior thermal topology of a given component in terms of an equivalent electrical network of varying complexity. Matrix representations are also used for more complicated parts. Two examples of possible compact model representations for a typical leaded package are shown in figure 1. The first approach depicts a 3D representation using blocks with effective properties, while the second approach depicts a typical network representation of the device linked to the printed circuit board.

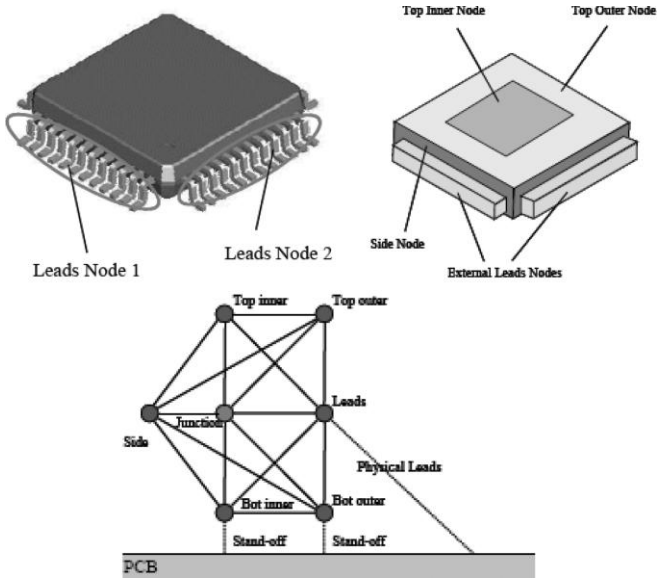


Figure 1 Examples of compact model formulations for a leaded package (courtesy JEDEC JC15.1).

Starting in 1996, PROFIT followed up the DELPHI project and this time had semiconductor manufacturers onboard. It continued and extended previous work and changed the character of these developments into collaboration between manufacturers and end users. SEED was the last of the European projects that started in 2000 and extended compact modeling into the transient domain. The foundations laid out by these three projects have been adopted by JEDEC, the semiconductor engineering standardization body of the Electronics Industries Association (EIA). The standards and methodologies behind CTM development and application continue to be actively pursued by JEDEC subcommittee JC15.1 whose charter focuses on thermal characterization of microelectronic packaging. For more information please see Guenin [2, 3].

The following methodology which has been proposed for developing compact models involves:

1. Creation of a calibrated detailed model of an electronic device. This full fidelity or detailed model typically is constructed using a CFD tool. The key feature here is to ensure mesh independence model predictions.
2. Exercising the detailed model for a broad set of boundary condition combination on encompassing all boundaries where significant heat transfer occurs.
3. Definition of the compact model layout. Define an appropriate thermal network representation of the device.
4. Definition of the objective function to be minimized in the optimization procedure
5. The actual optimization. By varying the parameters of the CTM, the user cost function is optimized. Any scheme is acceptable here, from least-squares approaches to Genetic Algorithms.
6. Evaluation of accuracy of the model. Typically done using two distinct and independent sets, a generating set and a test set to allow for Boundary Condition Independence (BCI).
7. Make the compact model available to end users of the device or hardware in question.

The salient features of the CTM developed under the JEDEC/DELPHI procedure are Boundary Condition Independence (BCI) and scalability of the process to more complex devices and systems. BCI here refers to the ability of the compact model to maintain acceptable accuracy in predicting the thermal behavior of the device for all physically reasonable forcing conditions.

The electronics industry experience has been a positive one. The adaptation of the JEDEC standards for the thermal characterization of common devices and components has

enabled equipment manufacturers to significantly reduce design-cycle time and physical prototyping.

Systems and hardware developed for military applications encompass a much broader range of thermal environments and significantly more complex hardware than the devices typically encountered in the industrial electronics component- packaging sector. Nevertheless, the benefits to the military complex industries could be as significant if an appropriate set of standards were developed and implemented across the industry. This will facilitate the development of reduced order models for hardware that can be made available to any legitimate end user integrating these components onto more complex systems. Modeling and Simulation already plays a fundamental role in the development of most modern pieces of hardware. Therefore, the detailed FEA or CFD models needed in developing suitable reduced order hardware performance characterization models are likely to already exist. The additional cost of taking the extra step and developing "compact" models is then limited to efforts needed in exercising the detailed FEA/CFD models to generate the required data.

DISSIPATER HARDWARE DESIGN

In the context of this study, an electrical energy dissipater is considered to be a device that coverts electrical power into waste heat. The system consists of an array of resistive elements that convert electrical energy into thermal energy (Joule heating) and dispose it to ambient environment. Several alternative design architecture options exist for achieving this goal. These include air-cooled resistive coils, direct liquid-cooled coils using a dielectric coolant such as oil, and passively or actively cooled solid storage units. The optimum design choice for the energy dissipater architecture for any given vehicle should be derived from the decomposition of system level requirements.

Dissipater Physical Architecture

The system under consideration in this study is a liquid cooled solid storage design. The key attributes of this type of a system are the high specific heat storage capacity and the ability to control the rate of thermal energy release into the cooling system thus minimizing the impact on cooling system hardware by preventing the peak cooling load demands from becoming excessively high.

A schematic of the dissipater system is shown in figure 2. The system consists of three resistive panels that covert the applied electrical power into waste heat that can be discarded into the ambient environment. The resistive panels are in direct contact with a liquid cooled chassis, or manifold, which facilitates heat rejection from the system. In addition to the three resistive panels, the energy dissipater system includes a high-current inductor which is beneficial to stabilizing the high-voltage bus from current ripples.

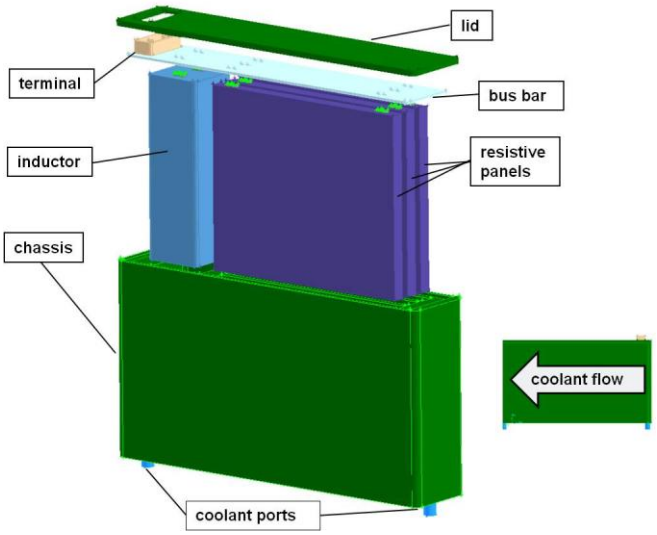


Figure 2 Typical Energy Dissipater System.

The dissipater panels consist of a resistor coil or wire, sandwiched between two substrates that provide the required electrical isolation from the high voltage and current flowing within the panel, while at the same time contributing to the overall thermal storage capacity of the system. A schematic of a typical construction for the type of resistive panel under consideration here is shown in figure 3.

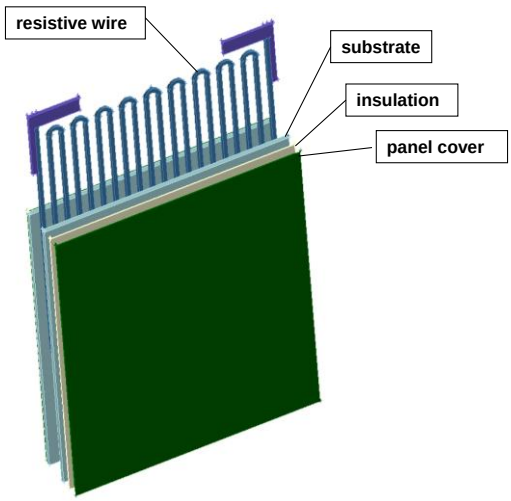


Figure 3 Dissipater Resistive Panel

Modeling and Simulation Support

Viewed from a thermal perspective, the operation of the dissipater during a short duration high-power event is quite straightforward and can be characterized by the following sequence of overlapping events:

- In the early stages of the event, the resistive coils start to get hot as a result of Joule heating. During this initial phase most of the energy associated with the event is primarily stored within the coils themselves.
- The heating of the coils triggers the onset of heat diffusion into the adjacent substrates. For relatively short duration pulses the heat storage within the substrates continuous to increase throughout the event.
- When the thermal front propagates through the substrates and past the exterior panel casing it triggers the onset of the cooling phase of the cycle characterized by controlled heat rejection from the thermal mass of the system into the coolant.

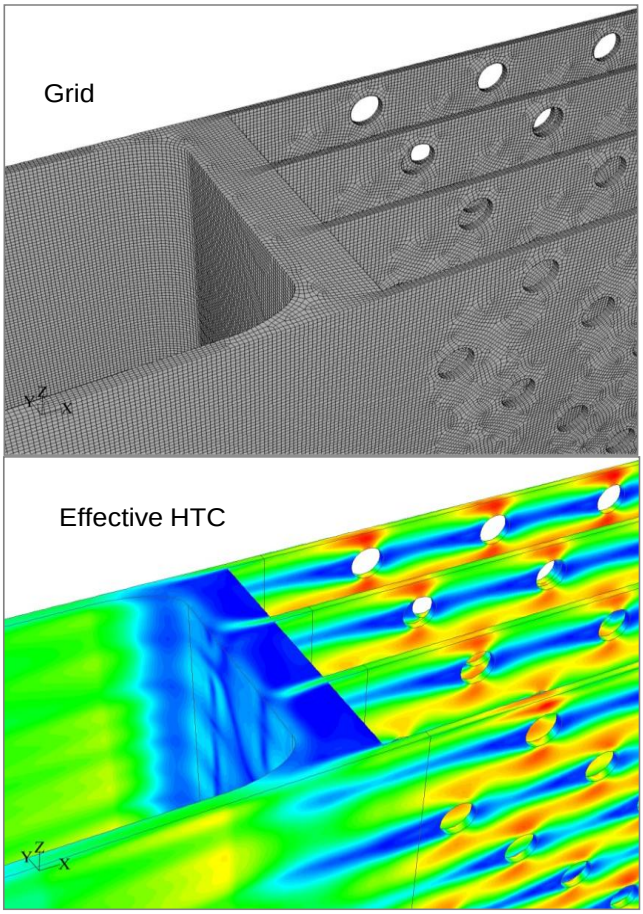
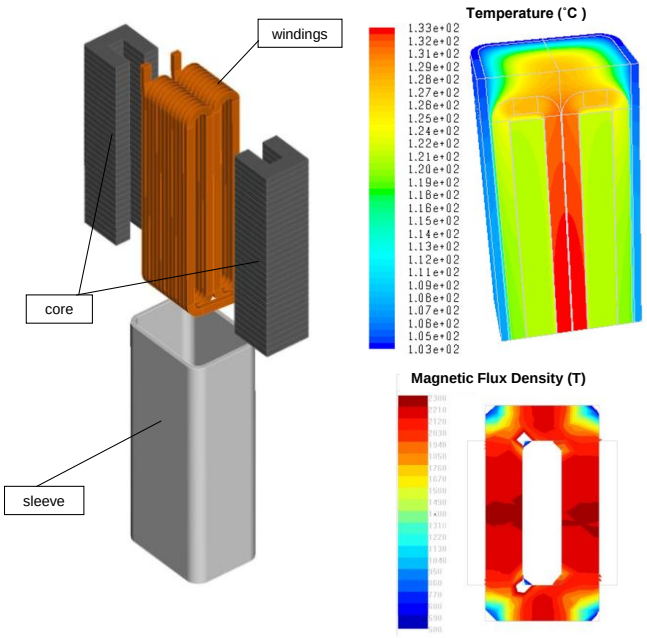


Figure 4 CFD Analysis of Dissipater Chassis

A Modeling and Simulation centric environment fosters the concurrent development of not only the hardware but also the associated performance simulation models needed to characterize it. A family of dissipater analysis models were constructed and used to support the hardware design and optimization.

Three-dimensional conjugate heat transfer CFD models based on the commercially available ANSYS/Fluent code were used to design and optimize the hydraulic and thermal performance characteristics of the energy dissipater system. These analyses help minimize the required coolant pressure drop, optimize flow distribution and flow uniformity across the system, and ensure that sufficiently high heat transfer rates could be maintained across a broad range of operating conditions, thus minimizing the dependence of the characteristic thermal time constant of the system on the flowrate and coolant inlet temperature. Sample results for the chassis CFD analysis are shown in figure 4. This includes a description of the computational mesh used for the calculation of the solution and a contour map of the effective heat transfer coefficients along the wetted surfaces of the outlet-side half of the dissipater chassis.

Non-uniformities in the local heat dissipation rate within the resistive coils were examined using a three-dimensional electromagnetic model based on the commercially available code ANSOFT/Maxwell 3D. The results from these analyses provided the necessary background to evaluate the thermal



impact of variations in the local heat dissipation rate within

Figure 5 Inductor Performance Characterization

the resistive coils brought about as a result of the local wire geometry. A separate electromagnetic model was used to perform the physical design and performance optimization of the dissipater power inductor. Sample results from the inductor analysis are shown in figure 5. This includes a schematic of the double-C laminated core inductor layout along with a temperature contour map corresponding to steady state operation of the device. Figure 5 also depicts the magnetic flux density lines on a mid-height plane cut through the inductor.

A sequence of structural analyses was performed using IDEAS and Nastran to ensure that the dissipater chassis design could withstand the shock and vibration environment typical of that encountered by ground combat vehicles. Stresses induced by thermal expansion effects and their impact on the fatigue life of the dissipater components were also carefully examined.

One of the key aspects of the thermal design of the dissipater system is the optimization of the wire/substrate interface which has a direct impact on the resulting effective power capacity of the system. Minimizing the thermal resistance of this interface enhances the diffusion rate from the wire to the surrounding substrate, which represents a substantially more efficient thermal storage medium than the wire. Optimization of this interface facilitates the design of systems with very high specific heat storage capacities. A suitable figure of merit, E, describing the effectiveness of the system to store thermal energy for a given event of characteristic time constant τ is given by:

$$E = \sqrt{(k\tau / \rho c_p)} \times (\rho c_p) = \sqrt{(\rho c_p k \tau)} \qquad (1)$$

Here, k is the thermal conductivity of the participating material, ρ denotes its density, while c_p is used to denote its specific heat capacity. The above equation represents the product of the thermal boundary layer penetration depth and the effective heat storage capacity of the material.

Both two-dimensional and three-dimensional thermal models were used to examine the dependence of the energy storage capacity of the system on the effective properties of this thermal interface. An array of carefully conducted tests provided a baseline for calibrating and validating the analytical interface models. The thermal response of the system following a 30 second event is shown in figure 6 and figure 7. The heating of the resistive panel due to the applied power is shown in figure 6 for eight distinct times spanning the actual event and the subsequent cool-down period. Changes in the overall energy storage of the system for the same event are shown in figure 7. Note that for this particular panel configuration, at the end of the power pulse

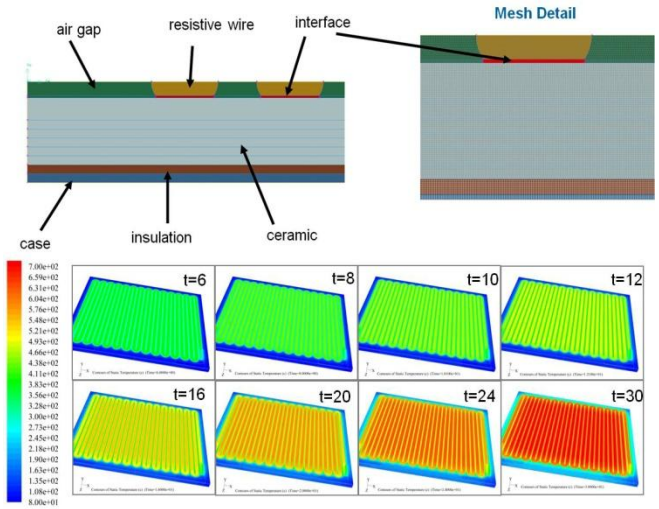


Figure 6 Electric panel response to high- power pulse

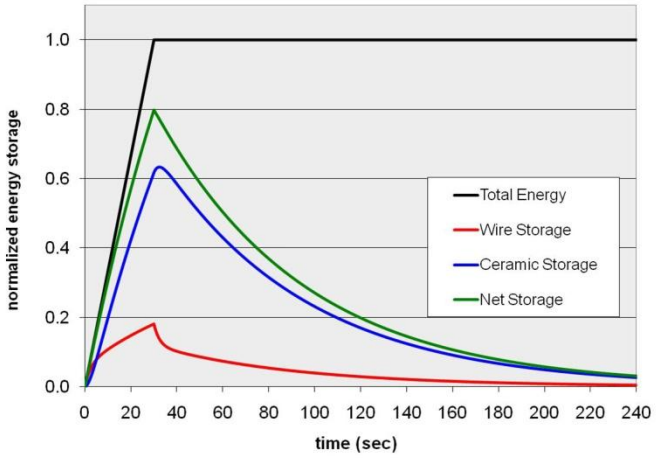


Figure 7 Thermal energy storage vs. time

less than 20% of the total energy dissipated by the system is stored within the resistor coil itself, while more than 60% contained within the substrate.

Another aspect of the dissipater thermal design is the thermal management of the heat generated and stored within the system during a high-power pulse event. Within a very short time interval following the onset of such an event, both the wire and the interior substrate temperatures could easily rise to levels several hundreds of degrees Celsius above the ambient. In order to prevent these elevated temperatures from reaching the liquid cooled manifold and possibly causing localized boiling of the coolant, the exterior surfaces of the substrates are thermally insulated. In addition to keeping the chassis wetted surface temperatures within acceptable limits, the panel thermal insulation also provides

means for controlling the thermal time constant of the system. Slowing down the rate of heat rejection into the cooling system mitigates the impact of the electrical dissipater operation on the vehicle peak cooling requirements which ultimately determine the sizing of the cooling pack.

System level performance analysis models provide the critical stage for simulating and understanding the behavior of the vehicle following the integration of numerous components and subsystems. Reduced order component models that are capable of running faster than real time when integrated in either software or firmware, also provide a platform for the diagnostic/prognostic monitoring and the control of the device when necessary.

A reduced order transient CTM capable of predicting the dissipater thermal response under a broad set of forcing conditions was developed and used to support vehicle level performance analyses and also to facilitate the dissipater controls development and implementation. A Discrete Thermal Model (DTM) formulation, derived from first principles, was used as the baseline for the development of the dissipater CTM. This formulation provides a one-dimensional finite difference representation of the entire thermal path through the system, starting from the centerline of the resistive wire and extending to the coolant flowing through the dissipater chassis. The thermal interface between the wire and the adjacent substrate is also explicitly modeled using a finite difference representation.

The CTM can be used as a standalone thermal simulation tool or it can be embedded into the Matlab/Simulink simulation environment. The dissipater CTM provides a time accurate prediction of the thermal response of the system for a given set of forcing conditions. Model inputs include the coolant flowrate pressure and temperature, and a power level command. At each integration step, the model updates the temperature at each interior node position. Approximately 80 interior nodes are used to define the temperature profile through the system. Model outputs include the maximum wire temperature, the outlet coolant temperature and pressure, and predicted temperatures at each of the RTD sensor locations. The model also calculates and reports the maximum available power dissipation level based on the current thermal state of the system.

The maximum wire temperature is one of the key metric in establishing the available capacity of the system to absorb additional power. Note that, based on the construction of the dissipater panels it is rather difficult to obtain an accurate and reliable wire temperature measurement either by direct or optical means. Consequently, the actual wire temperature is inferred through model predictions while measurements from sensors that are somewhat remotely located are used to monitor and control the run time accuracy of the CTM. The thermal model provides additional means for monitoring the capacity of the system to absorb power from the high voltage bus. An energy balance based on the First Law of Thermodynamics is initiated following the detection of the onset of a *significant* event and it is continuously tracked for duration of that event. This enables an active monitoring of the residual energy storage within the system and it provides means for adjusting the reported available dissipation rate.

DISSIPATER CONTROLS

The dissipater controls were developed with a high fidelity Matlab/Simulink model to operate robustly over a wide range of operating conditions along with significant system parameter variation. The control system was a simple nested configuration with an outer voltage regulation loop that commanded a coil current loop along with power limiting from the CTM model. The key to robust operation over a wide range of operating conditions was current mapping and gain scheduling as a function of bus voltage.

Simulink High-Fidelity Model

The dissipater controls model was built with Matlab/Simulink as shown in figure 8. The model consisted of subsystem models for controls, physical systems, disturbances and our in house sine sweeper. The subsystems contained a standardized interface of controls signals and physical signals in on the left, and controls signals, physical signals and data logging out on the right. Interconnection of all the subsystems was performed with *buses* and *goto/from* tags which substantially simplified the interconnection process.

The controls subsystems consisted of a voltage loop controller and current loop controller. The controllers consisted of PI controllers with anti-windup and gain scheduling to improve performance which will be discussed in the control architecture and controller performance sections. Inputs to the controllers consisted of user inputs for bus voltage regulation, bus current and the power limit from the dissipater CTM. In addition, physical system feedback signals were input consisting of the coil current and bus voltage measurement. Output from the controllers was the PWM command to the IGBT gate drive in the dissipater model.

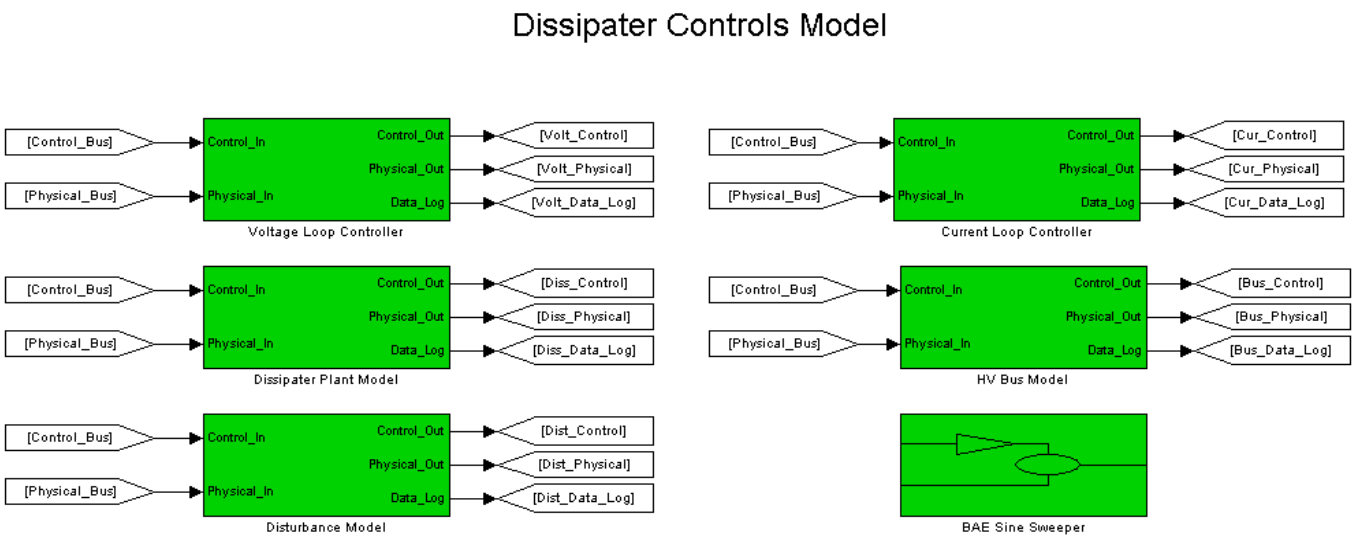


Figure 8 Dissipater controls coded in Matlab/Simulink

The physical system subsystems consisted of the dissipater subsystem and the high voltage bus subsystem. The dissipater subsystem contained the RL dissipater, IGBT approximation and dissipater CTM. The input to this model is the PWM signal from the current loop controller, and the outputs are coil current, bus current and dissipater power limit. Both current outputs deviate significantly at mid-power, which is the reason for the gain scheduling implemented in the voltage controller. The high voltage bus model was simply an RC model with the small inductance neglected. The input to this model was the dissipater bus current and disturbance current. The output of this model was bus voltage.

The dissipater disturbance subsystem consisted of a number of disturbances. Typical hybrid vehicle high voltage bus disturbances range from short transients to prolonged power dumps due to excessive regeneration. As a consequence, our disturbance model contained a number of worst case configurations for short period power pulses, along with prolonged continuous duty power dumps. The input to this model was the user selected disturbance and the output was bus current.

Finally, the BAE Systems sine sweeper subsystem was an in-house tool developed for analyzing non-linear control systems. This tool was built due to concerns with finite difference linearization tools. The sine sweeper physically injects a sinusoidal signal in the control system to determine magnitude and phase response as a function of frequency. This tool is used to determine open and closed loop bode diagrams which yield stability margins and closed loop bandwidth. The inputs to this model consist of an enable signal, sine source signal and sine response signal. The outputs of this model were magnitude, phase and frequency.

Control System Architecture

The control system architecture selected was a coil current loop nested inside a voltage regulation loop as shown in figure 9. This configuration was selected because it allowed for bus protection regulation along with power dumping capability. The bus protection regulation feature is used to regulate the high voltage bus at a voltage set point whenever the bus exceeds the capability of a regulator at a lower voltage set point. The power dumping capability via the current loop is used on occasion when power margin is required for high voltage bus protection.

The coil current loop consisted of an anti-windup PI controller with bus voltage gain scheduling. The anti-windup PI controller prevented the integrator from winding up excessively and allowed for a rapid recovery from saturation. The bus voltage gain scheduling was required to eliminate the dramatic change in loop gain that occurs from low to high voltage, since steady state coil current is:

$$I_{coil} = V_{bus} \frac{Duty}{R_{coil}} \tag{2}$$

As a consequence, gain scheduling consisting of $1/V_{bus}$ down to a limit of 10 volts for V_{bus} was implemented in the loop.

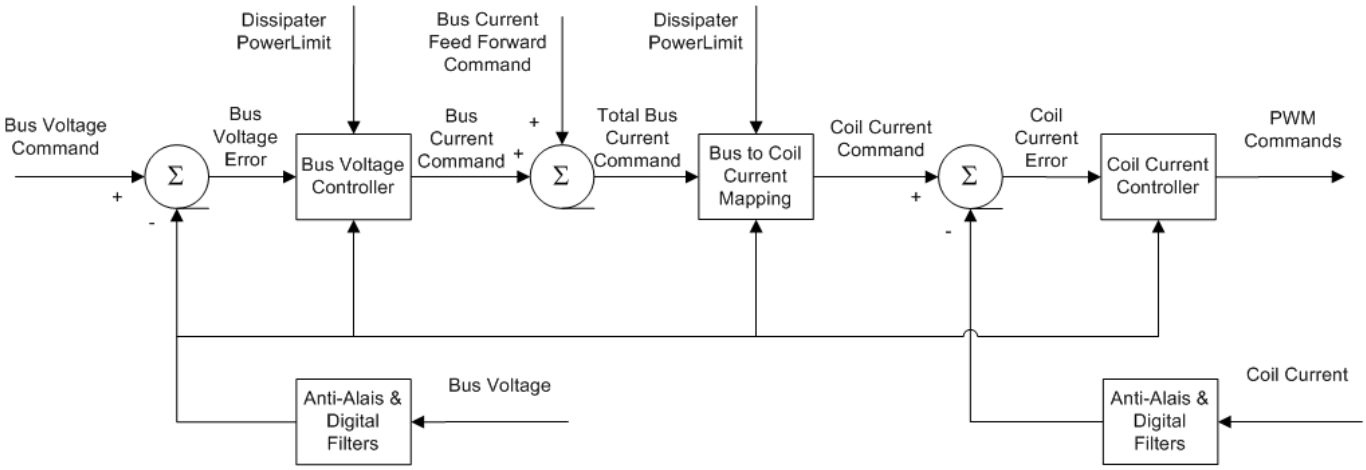


Figure 9 Control System Architecture

The voltage regulation loop consisted of an anti-windup PI controller with bus current to coil current mapping. The anti-windup PI controller was once again a PI controller, which prevented the integrator from winding up excessively. The bus current to coil current mapping eliminated the dramatic change in loop gain that occurred at various power levels and bus voltages. Mapping from bus current to coil current was accomplished with a simple steady state power equation,

$$V_{bus} \times I_{bus} = I_{coil}^2 \times R_{coil} \tag{3}$$

which in turn yields,

$$I_{coil} = \sqrt{\frac{V_{bus} \times I_{bus}}{R_{coil}}} \tag{4}$$

Control System Performance

The control system performance was determined from sine sweeping and step responses of the simulation model. Sine sweeps of the model were performed for both loop gain and closed loop configurations of the coil current loop and voltage regulation loop. Physical system parameters and operating points were varied to see their impact on stability margins and closed loop bandwidth.

The coil current loop was analyzed for loop gain performance and closed loop performance. The loop gain response with voltage gain scheduling was shown below in figures 10 and 11. The individual curves were of our baseline configuration along with extreme parameter variation for coil resistance and inductance. In addition, a range of voltages and coil current operating points were included. This allows us to check out nearly every possible configuration to find bounding limits. The tightly grouped curves had a crossover frequency of 375Hz to 523Hz with minimum gain and phase margins of 18dB and 75degs. The closed loop response was shown below in figure 12. The closed loop bandwidth was tightly grouped between 400Hz and 604Hz, which allows for a high bandwidth voltage loop.

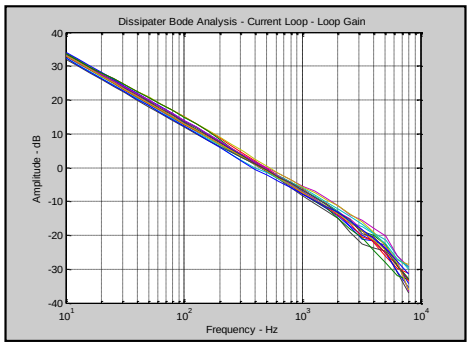


Figure 10 Coil current loop gain

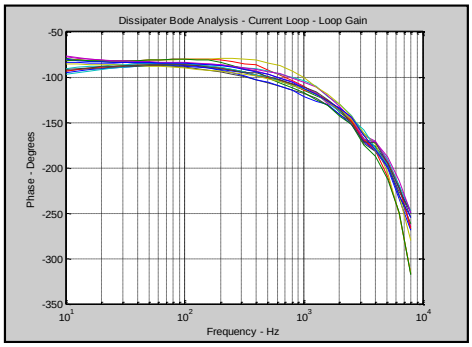


Figure 11 Coil current loop phase

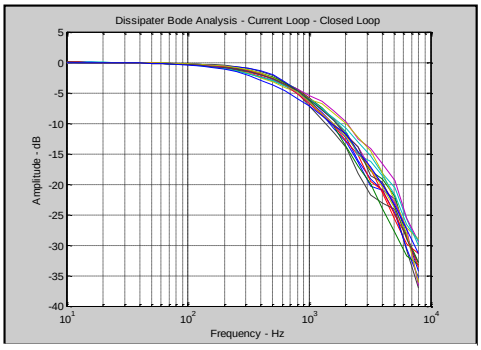


Figure 12 Coil current closed loop

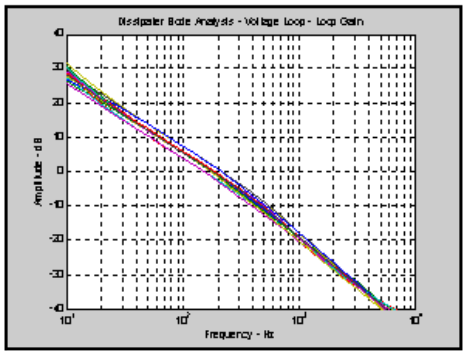


Figure 13 Voltage loop gain

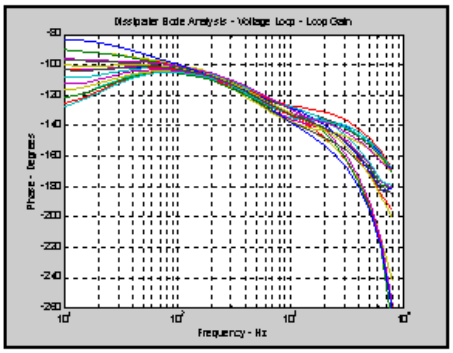


Figure 14 Voltage loop phase

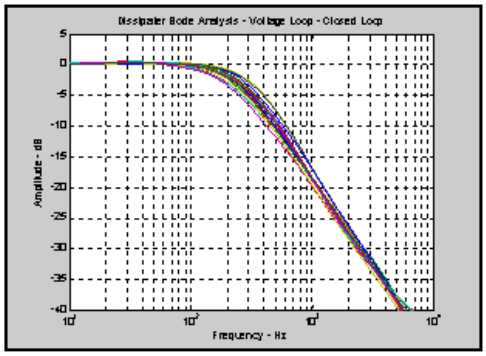


Figure 15 Voltage closed loop

The voltage regulation loop was analyzed next for loop gain performance and closed loop performance. The loop gain response with buss current to coil current gain scheduling was shown above in figures 13 and 14. The individual curves were of our baseline configuration, along with extreme parameter variation for coil resistance, inductance, bus resistance and bus capacitance. Variations in operating conditions consisting of bus voltage and bus disturbance were also included. The tightly grouped curves had a crossover frequency of 153Hz to 219Hz with minimum gain and phase margins of 35dB and 68 degrees. The closed loop response was shown below in figure 15. The closed loop bandwidth was tightly grouped between 189Hz and 319Hz which allowed for maximum bandwidth and good performance at all operating conditions.

Finally, a step response of the voltage loop along with disturbance steps were performed to see how the model performed in the time domain. We checked numerous configurations that would potentially be encountered. The voltage loop step, from operating voltage to zero as shown below in figure 16 is typically performed to discharge a HV bus with a time constant of 10ms. The disturbances steps ranging in magnitude up to max power as shown below in figure 17 are typical of regeneration events that require dissipation. The bus voltage is allowed to rise in these events from a regulated value to the set point of the dissipater (From 550VDC to 600VDC in this case). A maximum overshoot of 11% was acquired, which was key to prevent the bus voltage from triggering other controls which provide high voltage bus protection.

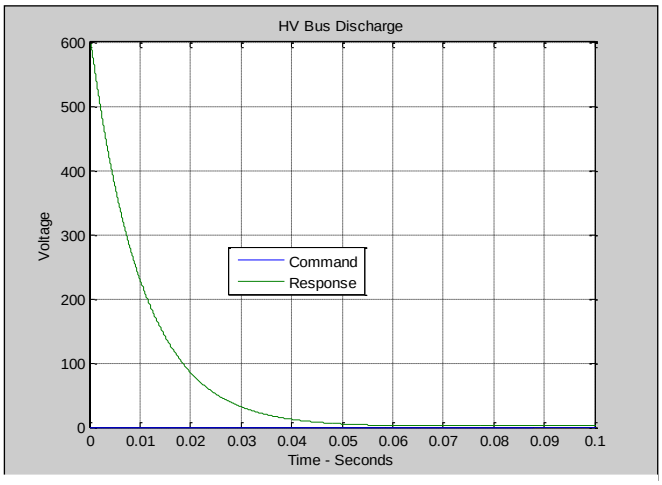


Figure 16 HV bus discharge

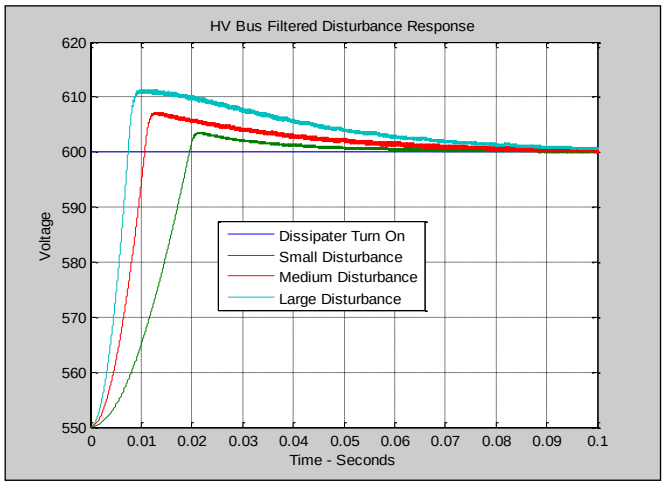


Figure 17 Disturbance responses

CONCLUSIONS

The use of physics based models to provide support and guidance throughout the hardware design and development phase for a typical piece of hardware, an electrical energy dissipater, has been described. The benefits of utilizing embedded models to provide a platform for the dynamic monitoring and control of the device have been presented.

Lessons learned from the electronics industry and the benefits of standardization have been briefly described.

The need to control escalating hardware development costs and to reduce hardware testing and fielding cycles ensures that Modeling and Simulation will continue to play an increasingly critical role in military hardware development. Models used to define, design, and develop hardware can easily be leveraged without the need for substantial additional investments to develop embedded reduced order models capable of capturing the behavior of the device in a dynamic environment. The standardization of the development process and the definition of a suitable model interface will lead to increased availability of such models, promising to greatly benefit the community as a whole.

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