2011 NDIA GROUND VEHICLE SYSTEMS ENGINEERING AND TECHNOLOGY SYMPOSIUM
POWER AND MOBILITY (P&M) MINI-SYMPOSIUM
AUGUST 9-11 DEARBORN, MICHIGAN

HIGH TEMPERATURE (250 °C) SIC POWER MODULE FOR MILITARY HYBRID ELECTRICAL VEHICLE APPLICATIONS

R. M. Schupbach, B. McPherson, T. McNutt, and A. B. Lostetter

Arkansas Power Electronics International, Inc.
535 W. Research Center Blvd.
Fayetteville, AR 72701
Phone: +1-479-443-5759
Email: mschupb@apei.net

John P. Kajs, and Scott G Castagno

Science Applications International Corporation
8303 N. MoPac Expy,
Suite B-450
Austin, TX 78759

ABSTRACT

In this paper, the authors present a line of newly developed high performance SiC power modules, HT-2000, for military systems and applications. The HT-2000 series of modules are rated to 1200V, are operational to greater than 100A, can perform at temperatures in excess of 250 °C, and can be constructed with SiC MOSFETs, JFETs, or BJTs. The newly developed module implements a novel ultra-low parasitic packaging approach that enables high switching frequencies in excess of 100 kHz, and weighs in at just over 100 grams (offering >4× mass reduction in comparison with industry standard power brick packaging technology). The paper discusses testing results of these modules in actual system applications, including: (a) complete static characterization vs. temperature, and (b) switching performance.

I. INTRODUCTION

The ever-increasing electrical power, power density, and cooling requirements of present and future military platforms are pushing silicon based power electronics system to its operational limits. To address future needs, wide bandgap semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) were developed for electronic applications. Using these semiconductor materials, a new generation of wide bandgap power devices is being developed. These new power devices offer characteristics and capabilities that are orders of magnitude improvements over their silicon counterparts, including 10× voltage blocking capability, 10-100× switching speed capabilities, $1/10^{th}$ energy losses, inherent rad-hard operation, and theoretical junction temperature operation up to 600 °C [1-2]. The impressive characteristic of this new power device technology could deliver power system with power densities as high as 10× of the present Si-based system in addition to minimum cooling needs, improved efficiency, as well as improved reliability.

Significant material and device advancements have been made over the past decade and power devices such as SiC Schottky diodes, SiC JFETs, SiC MOSFETs, and SiC BJTs are now commercially available from multiple companies such as Cree, SemiSouth, Rohm, and Infineon, among others [3-4]. The performance of these new devices is impressive; however, in order to develop of new power electronic systems that can achieve the envisioned goal for power density and efficiency goals, a new power module technology that maximize the performance of these devices is needed. Such new power module technology must have a number of important characteristics. First, it must be capable of delivering ultra-low parasitics that will enable high speed switching (10× over present technology). Second, it must be capable of reliable high temperature operation (250 °C and beyond). Third, this new power module technology must be capable of achieving ultra-high reliability. Lastly, to fully capitalize the advantage of this new power module technology a new gate drive technology as well as system level design techniques are imperative.

In this paper, a new line of high performance SiC power modules, HT-2000, is presented. The HT-2000 series of modules are rated to 1200V, are operational to greater than 100A, can perform at temperatures in excess of 250 °C, and can be constructed with SiC MOSFETs, JFETs, or BJTs.

The newly developed module implements a novel ultra-low parasitic packaging approach that enables high switching frequencies in excess of 100 kHz, and weighs in at just over 100 grams (offering >4× mass reduction in comparison with industry standard power brick packaging technology). Figure 1 shows a picture of the HT-2000 modules (left) along with the required busbar and gate driver (center and right). Section II discusses the module design philosophy as well as the design process. Lastly, section III presents static characterization vs. temperature and switching performance.

I. MODULE DESIGN

A Module Design Philosophy

Power electronic systems are diverse, with a wide range of applications, power levels, and environmental conditions complicating the selection of an appropriate module. As such, configuration flexibility is a very important feature. The HT-2000 line of power modules presented here was designed with this in mind and as such they are device neutral. This implies that the internal interconnection and layouts are compatible (or adaptable) with most currently or soon to be available SiC devices (MOSFET, JFET, BJT, etc.) from a variety of vendors. Newly available devices may be rapidly implemented in the housings with minor adjustments to the assembly process.

Power packaging for extreme environments presents significant challenges. As the operating temperature rises, the demands on traditional packaging materials surpass their limitations. Accordingly, the utilization of high temperature capable materials, attach processes, and minimization of coefficient of thermal expansion (CTE) differences must be the foundation of any such system. APEI, Inc. has embraced this challenge, aggressively developing extreme environment packaging solutions specifically for SiC and other wide band gap semiconductors. Power systems operating at junction temperatures ranging from 200 to 300 °C [5] and extreme environment sensor systems in a 450 °C ambient [6] have been demonstrated.

A second key design feature of HT-2000 series is the fact that it employs a novel interconnection scheme which allows it to be configured as either a half or full bridge configuration through external bussing. Figure 2 illustrates this approach. There are six external power connectors, two each for V+, V-, and output. For both configurations, the V+ nodes are shorted and the V- nodes are shorted. The difference is how the outputs are connected. Full bridge operation keeps the outputs separate, while half bridge connects them together. Independent gate and source kelvin signal pins allow for independent control of each quadrant.

A third key aspect in the design of the HT-2000 series is the manner in which parasitic impedances are handled. To start, the magnitude of the undesired path inductances are reduced through a number of techniques (covered in more detail in the respective sections for each module). While effective, parasitic impedances may never be eliminated, the layouts of these modules utilize a technique which ‘matches’ effective current paths to devices in parallel (including the path for the power and the gate drive signals). This reduces the effect of non-simultaneous switching events, where switches in parallel turn on in a cascading fashion, resulting in uneven current sharing among paralleled devices during high speed transition.

In [5], the authors demonstrated the benefits of matched power device layouts, performing a study comparing different methods to arrange six devices in parallel. Figure 2 (left) displays the turn-on current values for each device in a linear arrangement and (right) for a more symmetrical ‘forked’ arrangement with pairs of matched current lengths. By forking the layout, the current path length to the furthest

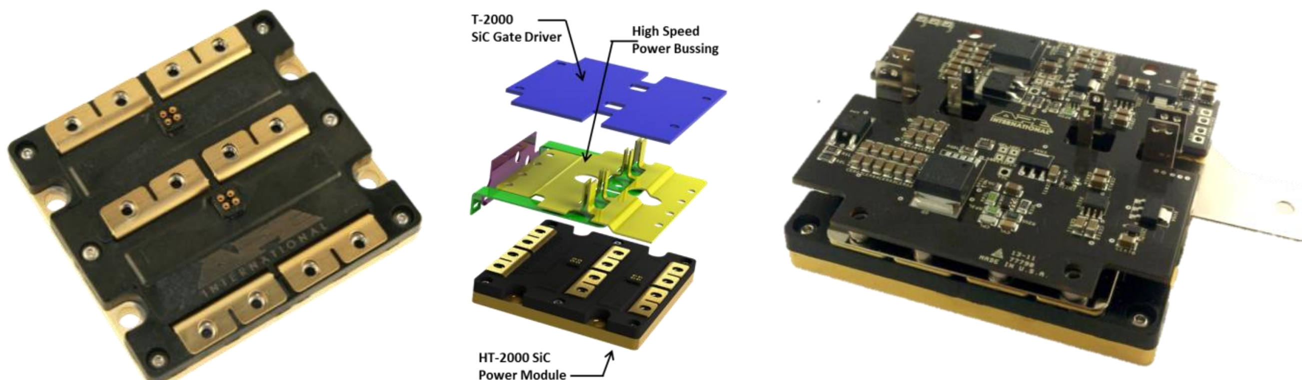

Figure 1. HT-2000 series module (left), module, gate driver and busbar assembly (center) and complete module assembly (right).

device is halved, and the burden is shared by two switches. This reduces the current peaks by nearly half, as well as halving the duration – resulting in a considerable reduction in switching loss. The HT-2000 series presented here takes this a step further, applying a novel layout which places devices in a complete parallel arrangement, allowing for simultaneous switching of greater than eight devices in parallel (per switch position) while all devices, in theory, sharing current equally under transient and dc conditions.

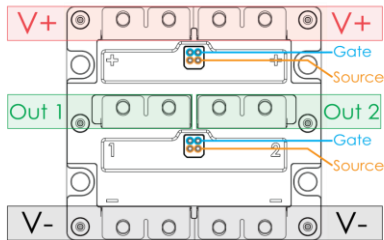

Figure 2. Flexible interconnection scheme of the HT series.

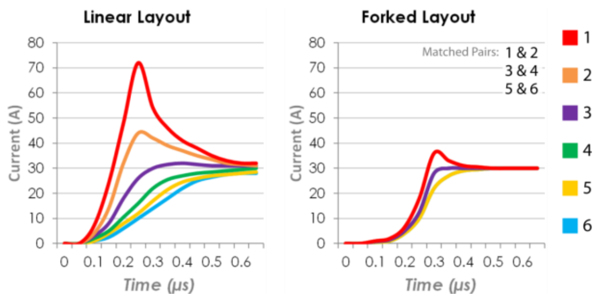

Figure 3. Parallel layout parasitic inductance effects on turn-on.

Another important aspect of the HT-2000 series is the fact that all components (i.e., substrate, devices, lead frames, etc.) are attached flux free with rugged high temperature solders, such as gold tin (80Au/20Sn), gold germanium (88Au/22Ge), and lead tin (95Pb/5Sn) alloys, depending on application. Eliminating flux from the assembly is important for long-term reliability. High temperature flux residues are difficult to clean, may corrode wire bonds or sensitive surfaces, and trapped vapors on large area bonds may leave large voids in the solidified bond line. Void free bonding is achieved with surface preparation via plasma cleaning of the joining surfaces and both sides of the solder preforms, precision assembly hardware, and customized reflow profiles in a vacuum/pressure reflow oven. Low profile heavy gauge power wire bonds are formed with a semi-automatic bonder with highly repeatable loop heights.

B Module Design Process

Many important, interrelated variables exist in the various functional elements of these modules. During the design phase, these factors were arranged into two groups: materials and geometry. Materials were outlined for the various components, including: base plate, power substrate metal, power substrate ceramic, external connection (lead frame, pins, etc.), housing, encapsulation/passivation, surface finish (plating, etc.), wire bonds, and solder attaches. Properties such as thermal conductivity, density, stiffness, and CTE were carefully outlined for each candidate material. The design of the HT-2000 series involved a detailed study of the base plate, power substrates material as well as various die attach materials among others. The importance of two of those components, namely die attach and base plate, is presented next.

When selecting an adequate die attach material, several key properties, besides melting temperature, must be carefully analyzed. It is also important to note that some of those properties may be heavily influenced by temperature. A good example of this is found in the die attach material; solders often have low thermal conductivities which can be heavily reduced at high temperatures (particularly as the solder approaches its melting temperature). Figure 4 presents a sweep of die attach thermal conductivity performed during the design of the HT-series module. Two high temperature solders (95Pb/5Sn and 80Au/20Sn) are highlighted, with the width of the region representing the range of the thermal conductivity from room temperature (upper limit of the region) to 250°C (lower limit). As shown, the die temperature is heavily driven by the attach conductivity at lower values. Interestingly, as the conductivity increases, the resulting die temperature experiences diminishing returns. Essentially, while significant thermal gains can be achieved by replacing a 95Pb/5Sn die attach with 80Au/20Sn at high temperatures, replacing the 80Au/20Sn alloy with a higher thermal conductivity alternative will not bring the same thermal benefits. It should be noted that the shape of this curve (including the rate of change and the location of the ‘knee’) is heavily driven by the rest of the system and is important to analyze for each particular design or configuration.

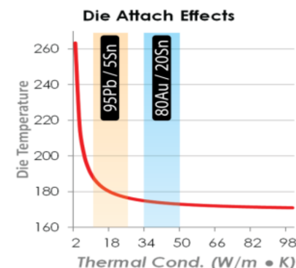

Figure 4. Effects of die attach thermal conductivity.

The selection of a good base plate material is a tradeoff between high thermal conductivities (metals such as copper

and aluminum) and low CTEs (alloys such as Kovar). One of the most effective compromises is to utilize advanced metal matrix composite (MMC) materials (copper moly, aluminum silicon carbide, etc.) which have CTE values which may be tailored to match the rest of the assembly while retaining a respectably high thermal conductivity.

The optimization of the module design requires the optimization of geometrical variables include base plate footprint, base plate thickness, power substrate metal thickness, power substrate ceramic thickness, solder attach thickness, device spacing, wire bond clearances, clearances for assembly hardware, vertical clearances, fastener locations, and lead frame geometry. To optimize the design, a set of Finite Element Analysis (FEA) simulation is carried out for each configuration. This requires the generation of a 3D model and the corresponding FEA mesh. With such a large number of variables, many of which are interrelated, optimizing a design for a target operating point can be extremely challenging.

An adaptive CAD modeling technique was used with the objective of to speed up the design process. To distill the large volume of data, 'sensors' are placed at regions of interest (die junctions, total weight, etc.) and may be outputted as charts. These are then analyzed and an informed, optimal solution may be determined that accurately weighs the tradeoffs. Each design variable is identified in the model, with interrelationships between components defined by geometrical relationships and equations. An excel file is linked to this model, tabulating the name and current dimension of each variable. If one value is changed, the entire assembly will rebuild itself automatically, resizing and rearranging each associated component as indicated by the defined relationships. As an example, if the space between devices is varied (to analyze the tradeoff between thermal spreading and module size), the power substrate, base plate, associated attaches, and die locations are all changed accordingly with no input from the user.

As an example, the design stage of the HT-series involved a detailed study of the base plate, carefully comparing multiple materials and geometrical configurations. One of the candidate materials, copper moly, is an excellent choice representing a high thermal conductivity (~190 W/m•K) and a low CTE (7.2 10-6/°C) with the drawback of a fairly high density (9.94 g/cm3). Analysis of this material included selecting a footprint that was small enough to house the required number of devices and interconnection while retaining an acceptable thermal performance and low deflection. Through adaptive CAD modeling, three dimensional surfaces for the die temperature (Figure 5, left) and peak displacement (right) were extracted. These simulation surfaces are invaluable in making effective design choices.

The resulting optimized module delivers a peak junction temperature capability of 250 °C, thermal resistance in the range of 0.09 to 0.13 °C/W (depending on power device selection) and a weight of 130 grams! This exceptional packaging performance has the potential of enabling the design of very high power density system.

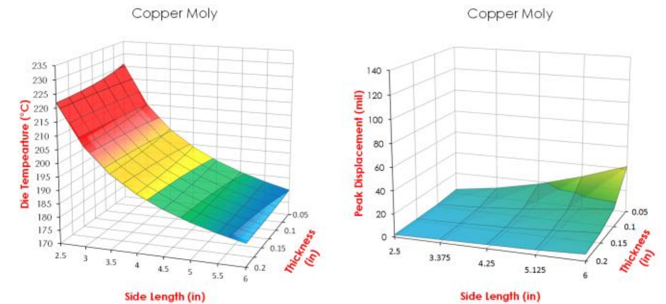

Figure 5. Example copper moly base plate design surfaces.

II. MODULE CHARACTERIZATION

The HT-2000 series module has been designed to accommodate a variety of SiC devices. Results presented in this section focus on two different modules, the HT-2000 MOSFET version and the HT-2000 JFET version. The HT-2000 MOSFET version is composed of three CMF20120D MOSFETs and two SDC30S120 diodes per switching position while the JFET version uses four SJEC120R050 JFETs and SDC10S120 diodes per switching position.

Figure 6 shows the on-state characteristics of JFET module (configured as half bridge) at 25 °C and 150°C. Higher temperature data (up to 250 °C) is presently being collected. Figure 7 (left) shows the JFET half-bridge module on-resistance vs. temperature at two different current levels for V_{GS} = 3.0V. Note the increase in on-resistance at higher current and temperature as the module begin to enter saturation. Figure 7 (right) shows the JFET half-bridge module trans-conductance curves for two different temperatures. A slight change in threshold voltage can be observed. Figure 8 shows the JFET half-bridge module turn on (left) and turn off (right) event for V_{DS} = 600 VDC and I_{DS} = 120 Amps at room temperature. This module delivers very impressive current and voltage fall and rise times completing switching events in under 50 ns. As shown in Figure 8, turn-on losses are smaller than turn-off losses. Due to the high speed of the turn-on event and the inductance associated within the module, little overlapping between voltage and current is observed (soft switching effect) greatly reducing the turn-on losses. In order to estimate the magnitude of the over-voltage, the test setup did not include

any snubber circuit. An overvoltage of only 180 V was observed while switching at the maximum speed.

Figure 9 (top) shows the on-state characteristics of MOSFET module (configured as half bridge) at 25 °C and 150°C. Higher temperature data (up to 250 °C) is presently being collected. Figure 9 (bottom) shows the MOSFET half-bridge module trans-conductance curves for two different temperatures. A slight change in threshold voltage and saturation current can be observed.

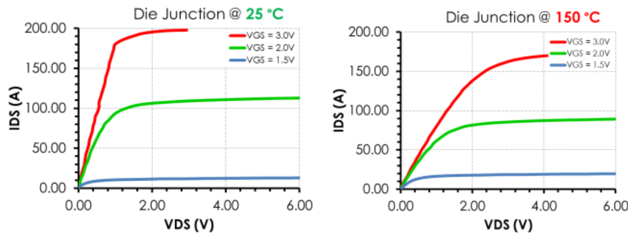

Figure 6. On-state characteristics of JFET module at 25 °C (left) and 150°C (right).

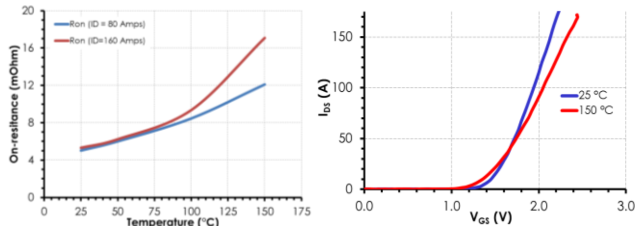

Figure 7. JFET module on-resistance vs. temperature at two different current levels for V_{GS} = 3.0 V (left) and half-bridge module trans-conductance curves for two different temperature (right).

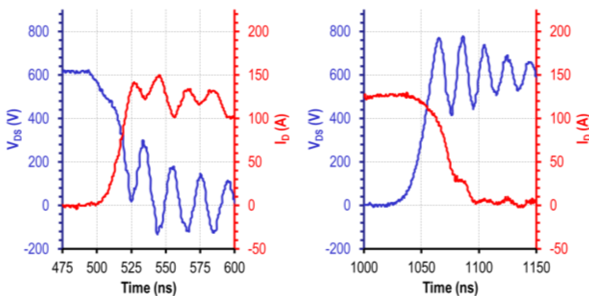

Figure 8. JFET half-bridge module turn on (left) and turn off (right) event for V_{DS} = 600 V_{DC} and I_{DS} = 120 Amps at room temperature.

Figure 10 shows the MOSFET half-bridge module on-resistance vs. temperature at two different current levels for V_{GS} = 20V. Note that while the on-resistance increases with temperature and current as expected, higher current and temperature measurements show no signs of clear saturation even at 200 Amps and 200 °C.

Figure 11 shows the MOSFET half-bridge module turn on (left) and turn off (right) event for V_{DS} = 600 V_{DC} and I_{DS} = 150 Amps at room temperature. As in the case of the JFET module, the MOSFET module delivers very impressive current and voltage fall and rise times completing switching events in under 50 ns. As in the case of the JFET module, turn-on losses are smaller than turn-off losses and due to the fact that high speed turn-on event yields little overlapping between voltage and current (soft switching effect). Figure 11 (right) show an import over-current spike during the turn-on event. This over current is not due to diode reverse recovery since SiC Schottky diodes are used but rather this is product of the rapid discharging of the switching position capacitance. The MOSFET module has an equivalent switching position output capacitance significantly larger than the JFET module. In order to estimate the magnitude of the over-voltage, the test setup did not include any snubber circuit. An overvoltage of only 180 V was observed while switching at the maximum speed of the module (0.0 Ohms gate resistance).

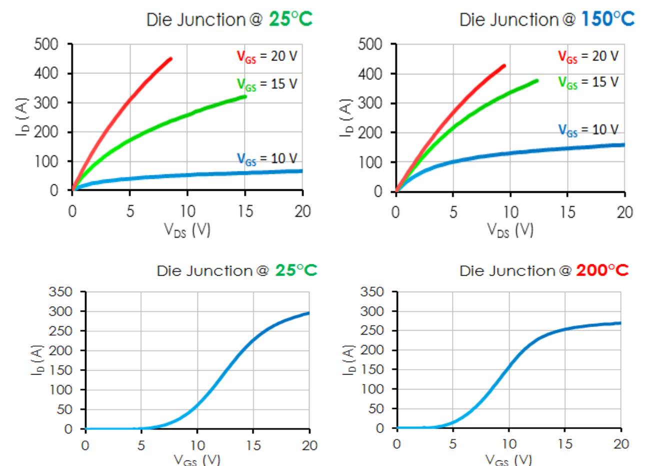

Figure 9. MOSFET module on-state (top) and trans-conductance (bottom) curves for different temperatures.

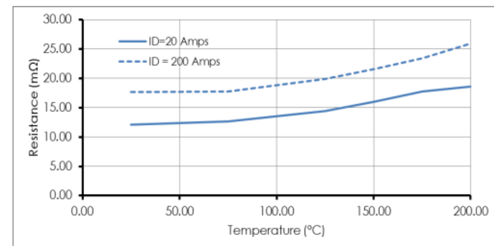

Figure 10. MOSFET module on-resistance vs. temperature at two different current levels for V_{GS} = 20V.

Figure 12 shows the total switching energy for MOSFET and JFET half-bridge modules vs. drain current for 300 V_{DC} (dash) and 600 V_{DC} (solid). These ultra-low switching

losses are largely achieved through the extremely fast switching speed, parallel layout techniques (equalizing parasitic impedances between devices for simultaneous switching), custom high speed gate drivers, and the efficient switching characteristics of these SiC devices. Higher temperature data (up to 250 °C) for each configuration is presently being collected and will be available upon request.

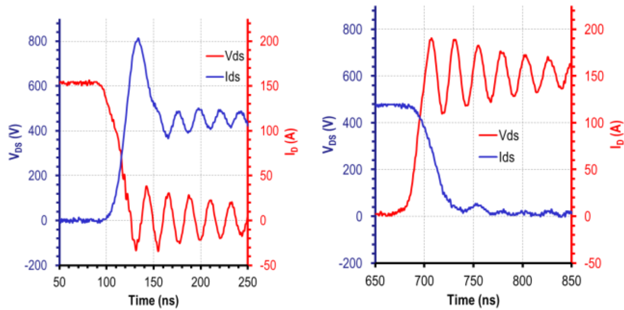

Figure 11. MOSFET half-bridge module turn on (left) and turn off (right) event for V_{DS} = 600 V_{DC} and I_{DS} = 150 Amps at room temperature.

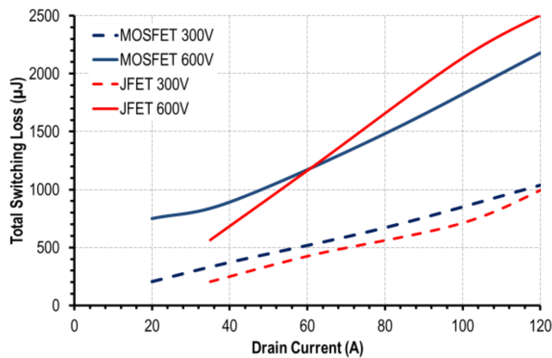

Figure 12. Total switching energy for MOSFET and JFET half-bridge modules vs. drain current for 300 V_{DC} (dash) and 600 V_{DC} (solid) condition.

Lastly Figure 13 shows some of the key feature of the HT-2000 series and how it compares to an advanced Si-based high-speed IGBT module. The new module delivers very impressive volume and weight savings while delivering very low switching losses and high temperature capability.

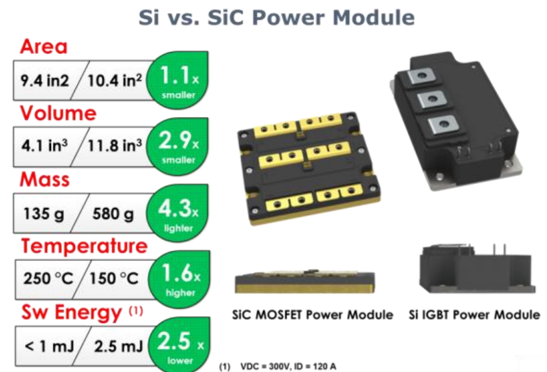

Figure 13. Comparison of HT-200 high power (1200V and >100A) SiC power module with state-of-the-art Si-based power modules.

III. SUMMARY

In this paper a new series of high temperature SiC power modules have been presented. This new module series, called HT-2000, was custom designed to take advantage of the unique benefits of SiC devices, including: high current density, high junction temperatures, fast switching speeds, and reduced losses.

Two variants of the HT-2000 series modules were also presented; each built with either JFET or MOSFET SiC devices (and associated SiC diodes). Characterization data was discussed for each (including on-state curves, on resistance vs. temperature, and switching curves). Lastly, ultra-low switching losses and extremely fast switching speeds (< 50 ns) were measured and demonstrated.

ACKNOWLEDGEMENTS

This material is based upon work supported by U.S. Army TARDEC under Contract Number W56HZV-10-C-0113.

REFERENCES

[1] A. Hefner, D. Berning, T. McNutt, A. Mantooth, J. Lai, R. Singh, "Characterization and Modeling of Silicon Carbide Power Devices", Semiconductor Device Research Symposium, Washington, DC, 2001.

[2] K. Shenai, R.S. Scott, B.J. Baliga, "Optimum Semiconductors for High Power Electronics", IEEE Transactions on Electron Devices, 1989.

[3] J. Richmond, S. Ryu, M. Das, S. Krishnaswami, S. Hodge Jr., A. Agarwal, J. Palmour, "An Overview of Cree Silicon Carbide Power Devices", Power Electronics in Transportation, 2004.

[4] P. Friedrichs, "Silicon Carbide Power Semiconductors – New Opportunities for High Efficiency", IEEE Conference on Industrial Electronics and Applications (ICIEA), Singapore, 2008.

[5] B. Reese, B. McPherson, R. Shaw, J. Hornberger, R. Schupbach, A. Lostetter, "High Temperature (250°C) Silicon Carbide Power Modules with Integrated Gate Drive Boards", International Conference on High Temperature Electronics (HiTEC), Albuquerque, NM, 2010.

[6] J. Yang, J. Fraley, B. Western, M. Schupbach, B. Keyes, J. Brogan, R. Geenlaw, "High Temperature Telemetry Systems for In-Situ Monitoring of Gas Turbine Engine Components", IEEE Aerospace Conference, Big Sky, Montana, 2009.