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A FAULT-TOLERANT HYBRID ELECTRIC VEHICLE POWERTRAIN

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Abstract

This paper presents a fault-tolerant powertrain topology for series hybrid electric vehicles (SHEVs). The introduction of a redundant phase leg that is shared by three converters in a standard SHEV drive system allows to maximize the reliability improvement with minimal part-count increase. The new topology features fast response in fault detection and isolation, and post-fault operation at rated power throughput. The operating principle, control strategy, and fault diagnostic methods are elaborated. The substantially improved reliability over the standard topology is verified by the Markov reliability model. Time-domain simulation based on a Saber model has been conducted and the results have verified the feasibility and performance of the proposed SHEV drive system with fault-tolerant capability. The experimental results from a prototype have further validated the robust fault detection scheme and excellent post-fault performance.

I. INTRODUCTION

Hybrid electric vehicles (HEVs), with their excellent mile-per-gallon performance, have been considered as a pivotal technology to mitigate concerns over the rapid rising of petroleum cost, increasingly worsening air pollution and global warming associated with greenhouse gas emission [1]. A literature survey conducted by the authors of this paper suggests that the major research effort has been focused on power electronic converter topologies and motor control systems related to HEVs while significantly less attention has been devoted to the reliability and fault mitigation of HEVs' powertrains. In fact, aggregation of many power electronic devices into drive systems of vehicles adversely affects reliability of the overall system [2]. The reduced reliability of HEVs not only discounts fuel-saving premium, but also increases repair time and maintenance cost. In light of safety concerns, faults that occur in electric drives for propulsion systems of HEVs can be critical since an uncontrolled output torque exerts adverse impact on the vehicle stability, which can ultimately risk the passenger's safety. Therefore, a fault tolerant operation even with partial functionality (commonly known as *limping-home function*) is desirable [3]. This paper compares and contrasts several candidates for fault-tolerant designs employed in HEVs electrical machine driving systems in terms of performance and cost. In [4-5], the authors present two types of switch-redundant fault-tolerant motor drive inverters with the feature of lower part count. However the dc-link capacitors have to be oversized to absorb fundamental load currents under faulted conditions. Consequently the post-fault maximum output power is reduced to such an extent that it renders the long-term operation impossible. The multi-phase motor drive inverter has inherent redundancy, but such a configuration is only suitable for motors with particular structure [6]. The authors of [7] present a four-leg motor drive inverter with redundancy, which does not require oversized dc-link capacitors and can provide the same peak output power under the normal and faulted conditions at the prices of higher cost. One common limitation among the aforementioned topologies is that they can only handle open-switch faults, while short switch is also a common failure mode that compromises reliable operation of motor driving systems [8]. The authors of [9] propose a new inverter topology for motor drives that is capable of dealing with open-switch and short-switch failures of the inverter. The main drawback of the scheme proposed in [9] arises from the high component-count of auxiliary devices and the associated higher cost.

A fault-tolerant electric drive system for series hybrid electric vehicles (SHEVs) is proposed to overcome the limitations that are associated with the existing topologies [10]. Based on performance metrics proposed in [11], the new topology can obtain the post-fault operation at rated power throughput with silicon-cost increase by 64% and seven ac switches compared with the standard topology. But only faults of IGBTs are included in [10]. In this paper, the faults of the anti-parallel freewheeling diodes are also investigated.

The rest of the paper is organized as the following. The operating principle of the proposed topology is explained in

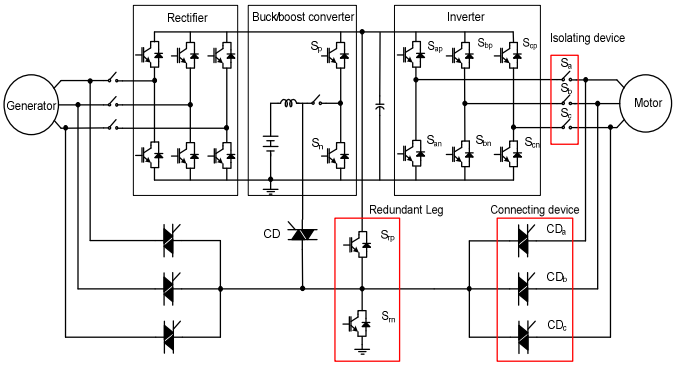


Fig. 1. Proposed fault-tolerant SHEV powertrain.

Section II. The salient reliability metrics of the existing and proposed SHEV powertrain are assessed and compared in Section III. Section IV presents the time-domain simulation results that verify the control of the proposed topology. A 5 kW prototype and the experimental results are presented in Section V. Finally, a summary and brief discussions conclude this paper.

II. Proposed SHEV Powertrain with Fault-Tolerant Capability

A standard SHEV drive system consists of a three-phase rectifier, a three-phase inverter and a bidirectional dc/dc converter. Faults on any power device can cause the system to shut down due to lack of redundancy. A fault-tolerant drive system for SHEV is proposed to reduce unexpected stoppages caused by faults of semiconductor devices. As shown in Fig. 1, the newly proposed system is composed of a standard SHEV powertrain, a redundant phase leg, connecting devices and fault-isolating components. The backup phase leg formed by S_{rp} and S_{rn} provides a redundancy not only to the motor-drive inverter, but also to the rectifier and the dc/dc converter. Under the conditions of open-switch or short-switch failure of any switch including switching devices and anti-parallel freewheeling diode in these three converters, the system can maintain an uninterruptible and long-term post-fault operation without compromising the power throughput. Since three converters share one redundant leg, the relative cost of the system is lower than other four-leg fault-tolerant inverters that have been reported in literature for motor drives.

A. Isolating and Connecting Devices

The short-switch fault is one of the most common types of motor driving inverter faults. In case of a short-circuit failure on any switch, one phase of the motor will be connected permanently to the positive or negative rail of the dc bus, which results in the pulsating electromagnetic torque. A device is needed to isolate the faulted switch from the overall system. Herein, an ac switch is utilized to fulfill this function. For instance, in the case that a short-circuit failure occurs on the upper switch S_{ap} of the *a*-phase leg of the inverter, the *a*-phase of the motor will be directly linked to the positive rail of the dc bus, as shown in Fig. 1. The resultant *a*-phase current becomes uncontrolled. After this fault is successfully isolated through turning off the switch S_a, further remedial measures can be employed to restore the normal operation of the system.

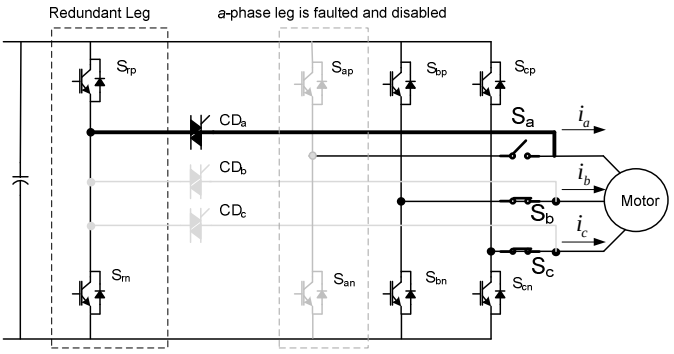


Fig. 2. Power circuit of the dc/ac part after its *a*-phase leg is faulted.

Since the inverter, the rectifier and the buck/boost converter share the same backup leg, a connecting device is necessary to connect the redundant leg to the output terminals. These devices need to block bidirectional voltage and conduct alternate current. Under post-fault operating conditions, the connecting devices for the inverter and the rectifier commutate once every fundamental cycle, so a low-speed low-cost ac switch suffices to handle this task. Although the buck/boost converter may operate in the discontinuous mode and consequently the connecting device has to commutate at the switching frequency, the same low-speed ac switch can still be applied to this converter as the connecting device, due to the inherent zero-current turning-off characteristic of the discontinuous-mode buck/boost converter. Herein, a TRIAC or double-thyristor connected in an anti-parallel manner is used to connect the backup leg to the poles of three converters.

B. Fault Types

Herein, each switch in the three power converters is composed of an IGBT and an anti-parallel freewheeling diode. The proposed topology can handle open-circuit and short-circuit faults of IGBTs and diodes in the three converters. The same control strategy for fault isolation can be applied to all these types of faults. Fault diagnostic methods for short-switch and open-switch faults are different.

Since the IGBT and diode are connected in anti-parallel manner, the short-circuit failures of the IGBT and diode result in the same configuration of the system. As a result, the short-circuit failures of the IGBT and diode can be detected by the same fault diagnostic method and termed as short-switch or short-circuit fault.

Unlike the short-circuit fault, it is more involved to identify the open-switch fault of the diode. When an open-circuit failure occurs to a diode, only the IGBT in the faulted switch is left. Since IGBTs only conduct unidirectional current, the inductive current that originally goes through the faulted diode has to charge the parasitic capacitor of the switch and leads to high emitter-to-collector voltage across the IGBT that can damages the IGBT. Therefore, an open-circuit fault in the anti-parallel freewheeling diode of an IGBT finally causes an open-circuit or short-circuit fault to the IGBT. Therefore, the open-switch fault of diodes can be identified by the fault detection/isolation logic of the IGBTs.

In the paper, the faults of IGBTs are mainly investigated, and the short-switch and open-switch faults refer to the faults of IGBTs.

C. Control Strategy

The proposed fault-tolerant solution shown features the unified fault isolation scheme for both short-switch and open-switch faults. The control strategy is briefly explained as follows. Once a fault in a switch is detected, the gating signals of the faulted and the healthy switches in the faulted leg are immediately disabled to prevent fault propagation. Then the corresponding ac switch is turned off to isolate the faulted leg from the rest of the system. Upon successful isolation of the fault, the corresponding connecting device is permanently triggered and the original gating signals of the faulted leg are routed to the corresponding switches in the redundant leg. Therefore, the redundant leg fully replaces the faulted leg and the system transits to post-fault operation that has the normal performance. The transition process of the system in the case of a fault is further illustrated with a short-switch failure to the top switch S_{ap} in the *a*-phase leg. When the short-circuit failure of the switch S_{ap} is detected, the controller immediately disables the gating signals of both switches S_{ap} and S_{an}. In the meantime, the ac switch S_a is turned off and the connecting device CD_a is turned on. Then the original gating signals of S_{ap} and S_{an} are utilized to control the switches S_{rp} and S_{rn} in the redundant phase leg. The normal operation of the drive system is resumed. Fig. 2 shows the reconfigured power circuit of the inverter after one switch of the *a*-phase leg fails. After the redundant leg replaces the faulted *a*-phase leg, the post-fault topology is identical to the standard three-phase inverter bridge except for the addition of the connecting device CD_a. The same transition steps can be applied to open-circuit faults of the switch and faults of switches in other phase legs and other converters.

D. Fault Diagnosis

Fault detection and identification are two important steps to prevent fault propagation and to maintain proper post-fault operation of the system. Table I shows the logic of fault diagnosis for the upper switch S_{ap} in the *a*-phase leg of the inverter. Herein it is assumed that a switch consists of an IGBT and an anti-parallel diode. It is worth noting that in Table I, when the current flows through the anti-parallel diode of a switch, the current through the switch is assumed to be at low level.

The principles of the diagnosis method are elaborated as follows. If the gating signal to a switch is at low level, while the sensed current through the switch is at high level, a short-circuit failure is thus asserted. In order to avoid false detection caused by the turn-off delay of IGBTs, the gating signal of the lower switch S_{an}, which is complementary to that of the upper switch S_{ap}, is utilized to detect short-switch faults. For conventional short-circuit protection, the design of the threshold of the current is a challenging task. A lower threshold for short-circuit detection logic will increase sensitivity of detection circuit but may lead to high possibility of misjudgment. On the contrary, while raising the threshold enhances the reliability of the fault diagnosis, the fault detection circuit is less sensitive to faults and a large inrush current may be generated before the short-circuit protection actuates.

TABLE I. FAULT DETECTION LOGIC OF S_{AP}

Driving signal of S_{ap}	**Driving signal of S_{an}**	**Voltage across S_{ap}**	**Current through S_{ap}**	**Fault detection**
High	/	High	/	S_{ap} OC fault
/	high	/	High	S_{ap} SC fault

The proposed diagnosis method for a short-switch fault will properly function within a wide threshold range as explained in the following. The proposed diagnosis logic for short-circuit faults is based on the fact that the current through a switch (IGBT) should be zero when the gating signal of the switch is at low level and that a short-circuit fault is certain if the switch current is non-zero given a low-level gating signal. Therefore, the current threshold can be much lower than the maximum operating current under normal operating condition. The effectiveness of the method is not affected by load conditions. For instance, in light-load condition or the neighborhood of the load current's zero-crossing point, the current flowing through the switch will still increase to the threshold of short-circuit fault diagnosis circuit in the case of short-switch fault. Since the switches are identical, the scheme of fault diagnosis can be applied to other switches as well.

The diagnosis logic for an open-switch fault is based on the gating signal and the collector-to-emitter voltage V_{ce} of a switch (IGBT). The open-circuit fault that occurs to the upper switch S_{ap} of the *a*-phase leg is taken as an illustrative case. Under the normal operating condition, when the gating signal to S_{ap} is high, the voltage V_{ce} across the switch S_{ap} must be at low level. Otherwise, if the voltage V_{ce} of the switch S_{ap} is at high level when its gating signal is at high level, an open-circuit fault is certain to occur to S_{ap}. An open-switch fault is asserted.

III. RELIABILITY ANALYSIS OF THE FAULT-TOLERANT SHEV POWERTRAIN

The reliability of the system is closely related to the repair cost and repair time. This section quantitatively assesses the reliability of the proposed and the standard SHEV drive systems. In the assessment of the new drive system's reliability improvement, semiconductor devices IGBTs, diodes and TRIACs, and relays are considered to demonstrate the methodology although inclusion of other passive components is rather straightforward.

A. Components Failure Rates

The reliability handbook MIL-217F [12] provides an extensive database of various types of parts. Therefore it is widely accepted and frequently utilized to determine reliability of various electronic equipments. In order to make use of the failure rate models of components from the handbook, the following operating conditions have been assumed.

1) The junction temperature of semiconductor devices is 150 ℃, and 100 ℃ for relays.
2) Failure rates of components in inactive mode equal to zero.

The reliability model of TRIAC is determined by

$$\lambda_{TRIAC} = \lambda_b * \pi_T * \pi_R * \pi_S * \pi_Q * \pi_E \quad (3)$$

where λ_b is base failure rate; π_T is temperature factor that is based on the junction temperature of a device; π_R denotes current rating factor that is determined by the rated current of the device; π_S is voltage stress factor that depends on the ratios of the applied block voltage to the rated block voltage of TRIAC; π_Q is quality factor; and π_E is environmental factor that models the effect of environmental stresses.

The MIL-HDBK-217F contains no reliability data about IGBTs. In consideration of the similarity between the internal structures of IGBTs and MOSFETs, the failure rate model of MOSFTs is chosen to estimate failure rates of IGBTs. Hence, the failure rate of IGBT can be expressed as

$$\lambda_{IGBT} = \lambda_b * \pi_T * \pi_A * \pi_E * \pi_Q \quad (4)$$

where π_A is application factor while the other parameters have the same meanings as those of the TRIAC reliability model.

The diode's failure rate model is determined by

$$\lambda_{diode} = \lambda_b * \pi_T * \pi_S * \pi_C * \pi_Q * \pi_E \quad (5)$$

where π_C is contact construction factor, while other factors are the same as those of the TRIAC and IGBT failure models.

The solid-state relay is utilized, and its failure rate model is

$$\lambda_{relay} = \lambda_b * \pi_Q * \pi_E \quad (6)$$

where π_Q and π_E are quality factor and environmental factor, respectively.

Based on the previously assumed operating conditions, known environmental and application conditions, the failure rates of IGBT, diode, TRIAC, and relay are evaluated and listed in Table II.

B. Reliability Evaluation of the SHEV Driving System

At the system level, Markov chain [13] is an effective approach to evaluating the reliability of fault-tolerant systems. This approach can cover many features of redundant systems such as sequence of failures, failure coverage and state-dependent failure rates. Markov model can be utilized to estimate various reliability metrics such as failure rate, mean time to failure (MTTF), reliability, and availability among others.

Herein, Markov reliability model is adopted to assess the reliability of the fault-tolerant SHEV drive system. In order to reduce the order of the state equation and simplify the analysis, all devices with the same operating states and transition processes are treated as one subsystem. The system can be divided into two subsystems: one including all IGBTs and diodes, and the other consisting of TRIACs. Repair processes have not been considered in this study. The system has three states:

State 0: All devices work well, and the redundant and connecting devices are in inactive mode;

State 1: One switch (IGBT, diode, or both) fails, and the redundant leg and correspondent connecting device TRIAC is activated;

State 2: two components (IGBTs or TRIAC or in combination) fail, and the system shuts down.

TABLE II. FAILURE RATES OF COMPONENTS

Component	Failure Rate	Unit
IGBT	39.798	Failure per 10^6 hours
TRIAC	4.693	
Diode	4.938	
Relay	0.661	

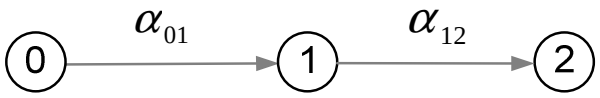


Fig. 3. State transition diagram of the proposed SHEV powertain.

The state transition diagram of the system is illustrated in Fig. 3. A short-switch or open-switch failure of any one of the IGBTs in the rectifier, the inverter or the dc/dc converter leads to transition of the system to state 1 from state 0. The transition rate α_{01} is the sum of failure rates of all operating IGBTs, diodes and relays, which can be expressed as

$$\alpha_{01} = 14(\lambda_{IGBT} + \lambda_{diode}) + 7\lambda_{relay} \quad (7)$$

Transition between state 1 and state 2 are triggered by a failure of one IGBT in remaining healthy and the redundant legs or the TRIAC that is in active mode. The transition rate α_{12} comprises the failure rates of operating IGBTs, diodes, TRIAC, and relays. It is worth noting that only one TRIAC operates in state 1. α_{12} can be determined by

$$\alpha_{01} = 14(\lambda_{IGBT} + \lambda_{diode}) + 6\lambda_{relay} + \lambda_{TIRAC} \quad (8)$$

The state equation of the SHEV system can be obtained

$$\begin{bmatrix} -\alpha_{01} & 0 & 0 \\ \alpha_{01} & -\alpha_{12} & 0 \\ 0 & \alpha_{12} & 0 \end{bmatrix} * \begin{bmatrix} P_0(t) \\ P_1(t) \\ P_2(t) \end{bmatrix} = \frac{d}{dt} \begin{bmatrix} P_0(t) \\ P_1(t) \\ P_2(t) \end{bmatrix} \quad (9)$$

Since the reliability of the system is the sum of the probabilities that the system is in the functional states at time *t*, the reliability function of the system can be obtained

$$R(t) = P_0(t) + P_1(t) \quad (10)$$

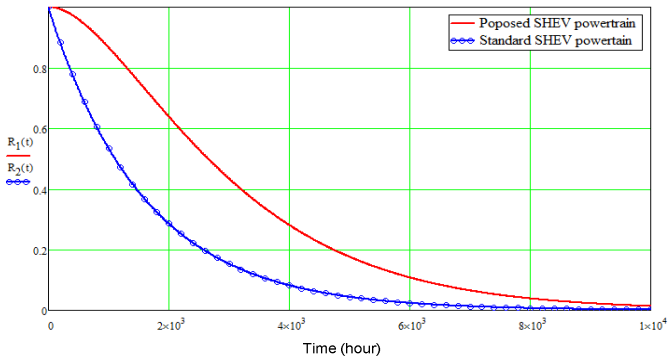


Fig. 4. Reliability functions of the proposed vs standard SHEV powertrains.

TABLE III. MTTF OF THE PROPOSED AND STANDARD SHEV POWERTRAIN

Topology	MTTF
Standard powertrain	1597 hours
Proposed powertrain	3160 hours

Fig. 4 illustrates the reliability functions of the proposed and the standard SHEV drive trains. It is evident that the reliability of the proposed drive system is much higher than that of the standard one due to the presence of the redundant phase leg.

The mean time to failure (MTTF) is another important index indicating the reliability of a system, which is closely related to the reliability function by the following,

$$MTTF = \int_0^\infty R(t)dt \tag{11}$$

In Table III, MTTFs of the new fault-tolerant and the standard SHEV drive trains are listed. The significantly improved MTTF demonstrates the super reliability performance of the new topology, since its operating time without disturbance is greatly improved to twice as much as that of the standard one.

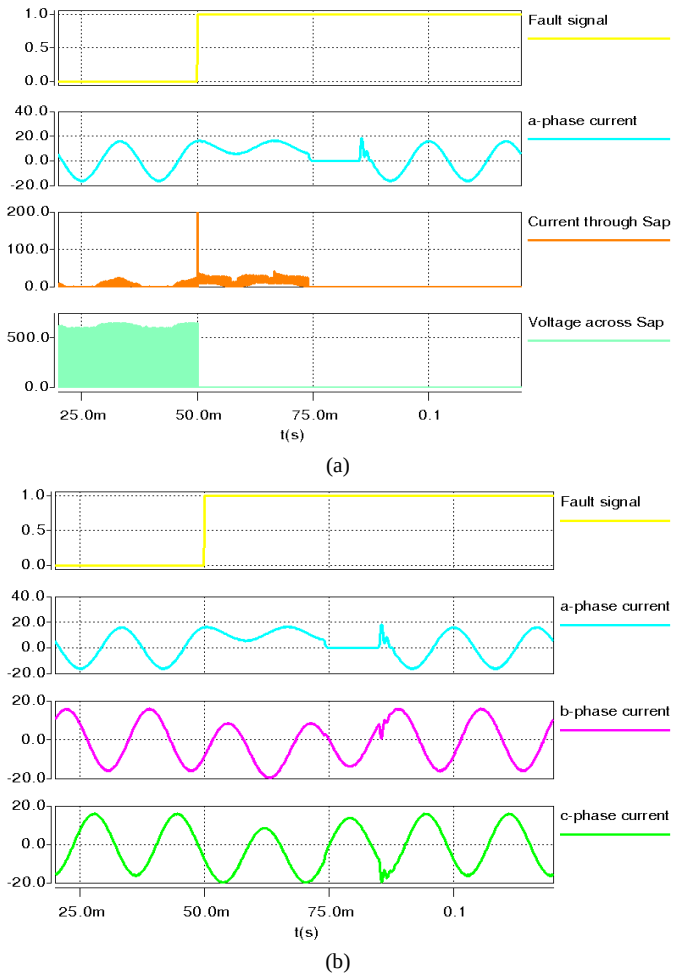


Fig. 5. Simulation results in case of short-switch fault S_{ap}: (b) the fault signal, the load current of the faulted phase, the current through the faulted switch, and the voltage across the faulted switch; (a) the fault signal and three-phase currents.

TABLE IV. SPECIFICATION AND PARAMETERS OF SIMULATION MODEL

dc-link voltage	600 V
Fundamental frequency	60 Hz
Switching frequency	5 kHz
PWM technique	SPWM
Modulation index	0.95
Load resistance	18 Ω
Load inductance	1 mH

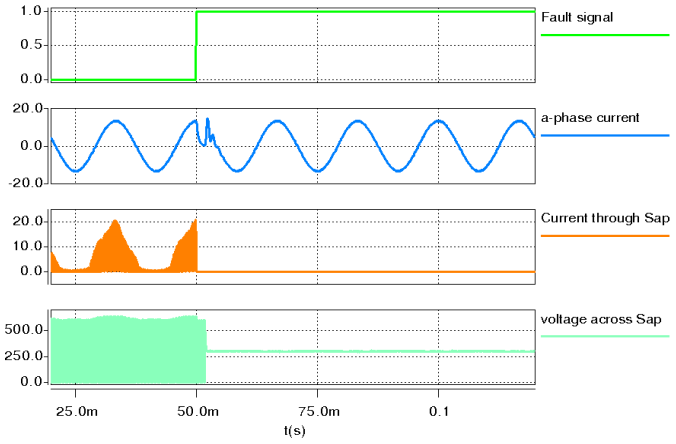
IV. SIMULATION RESULTS

The post-fault operating performance of the proposed SHEV driving system is verified by time-domain simulation. The simulation is based on the fault-tolerant design of SHEV powertrain as shown in Fig. 1. Because the fault diagnosis scheme and post-fault remedial strategy are identical for the inverter, the rectifier and the dc/dc converter, only the faults on the dc/ac inverter that directly drives the motor and the corresponding post-fault performance are investigated. The simulated system model consists of the proposed fault-tolerant three-phase inverter and a resistance-inductance load. The detailed specification and parameters of the system are tabulated in Table IV.

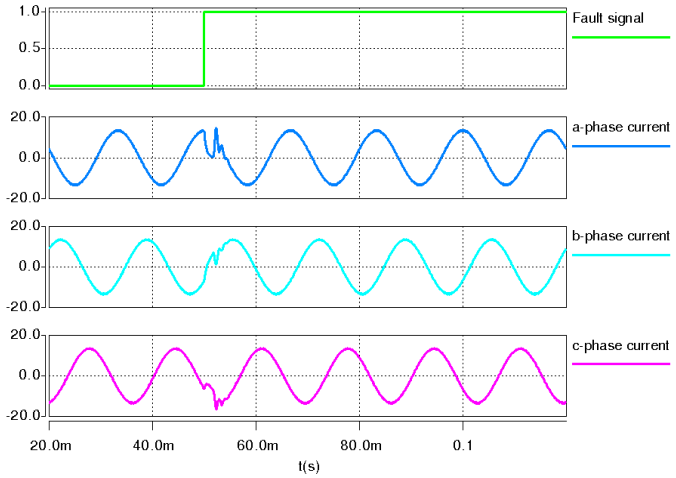
Fig. 5 shows the transition process of the system from the normal operating condition to short-switch fault condition of the inverter. At the instant of 0.05s, a short-switch fault occurs to the upper switch S_{ap} of the *a*-phase leg. A much-larger-than-normal current through the faulted device substantially results, as shown in Fig. 5(a). The immediate remedial action should be taken to avoid fault propagation.

The fault-detection method presented in this paper features a very short delay of approximate 200 ns that is caused by the analog components and a low-pass filter in the fault-detection circuit. At time instant t = 50 ms, a short circuit occurs to S_{ap}. Once the fault is detected, the gating signal of the bottom switch S_{an} in the *a*-phase leg is disabled and the large current flowing through the faulted leg during the interval of fault is immediately terminated, as shown in Fig. 5(a). Then the isolating device S_a is controlled to be open, and the connecting device CD_a is triggered. At time instant t = 74 ms, the relay S_a is fully disconnected. And in another delay of about 11 ms, the original gating signals to both switches of the faulted leg are routed to the corresponding switches of the backup leg at t = 85 ms. Herein, the delay between time instants t = 74 ms and t = 85 ms is inserted to guarantee that the relay is fully disconnected before the redundant leg participates in operation of the system. Otherwise, the bottom switch S_{rp} in the redundant leg and the faulted switch S_{ap} will form a shoot-through path. The post-fault operation starts and normal system performance is resumed from t = 85 ms, as shown in Fig. 5(b).

The transition process of the open-switch fault is illustrated in Fig. 6. The fault isolation actions taken by the controller are the same as the ones for the case of the short-switch fault except that the fault-detection logic is different, which has been explained in Section III. For the open-switch fault, since there is no concern about shoot-through path that formed by the faulted



(a)



(b)

Fig. 6. Simulation results in case of open-switch fault S_{ap}: (b) the fault signal, the load current of the faulted phase, the current through the faulted switch, and the voltage across the faulted switch; (a) the fault signal and three-phase currents.

switch and one switch in the redundant leg, the redundant leg can be enabled immediately after the redundant leg is disabled. Herein, the delay time between disabling the faulted leg and enabling the backup leg is set to 1.8 ms. Therefore, the disturbance of the system in the case of the open-switch fault is greatly reduced.

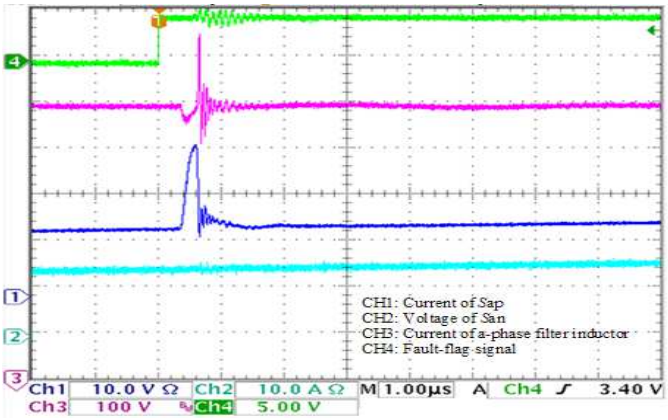
V. Experimental Results

A 5 kVA prototype of a three-phase inverter based on the fault-tolerant topology as shown in Fig. 1 has been built. The parameters of power circuit are the same as those of simulation model, as shown in Table IV. IGBT modules with anti-parallel diodes consist of main switches and connecting devices, and a relay with the release time of approximate 24 ms is used as fault-isolating component. The dc-link voltage is set up by a dc power supply. Three electronic loads are used as loads of the inverter. The LC filter is inserted absorb switching-frequency ripple so that the electronic load can normally operate.

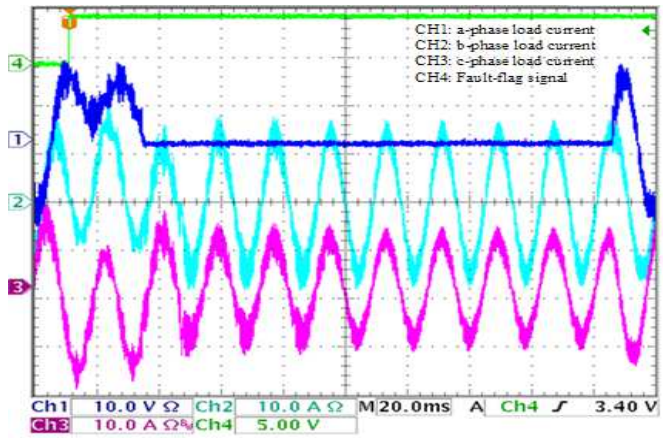
Fig. 7 demonstrates the fault transition process of the inverter for the short-switch fault of S_{ap}. At the rising edge of the fault signal, the gate-to-emitter voltage of the upper switch S_{ap} is forced to be constantly high, so that a short-switch fault occurs to S_{ap}. After about 400 ns turn-on delay, the switch S_{ap} is turned on, and the short-circuit path consisting of the dc-link capacitor and two switches in the faulted leg forms, and the fault current flowing through the faulted switch S_{ap} increases dramatically, as shown in Fig. 7(a). Then the fault is identified, and the gating signals to the switches in the faulted leg are disabled. As a result, the fault is cleared, the fault current disappears. It can be observed that the fault only approximately lasts approximately 200 ns, and the short-switch current that flows through the faulted switch is only approximate 31 A. It further verifies the fast response of the proposed fault detection method.

Since it takes approximate 24 ms for the relay to fully disconnect, the delay time of 35 ms between identifying the short-switch fault and enabling the redundant leg is inserted to prevent a short-circuit path formed by the faulted switch and the complementary switch in the backup leg. From Fig. 7(b), after approximate 100 ms, the load currents restore into normal operation. The disturbance time is mainly caused by the connection time of the electronic loads rather than by the control strategy. In the case of motor, the disturbance time is determined by the delay time between detecting short-switch fault and enabling redundant leg and can be greatly shortened.

Fig. 8 shows the fault transition process of the inverter in the case of an open-switch fault to the top switch S_{ap} of the inverter

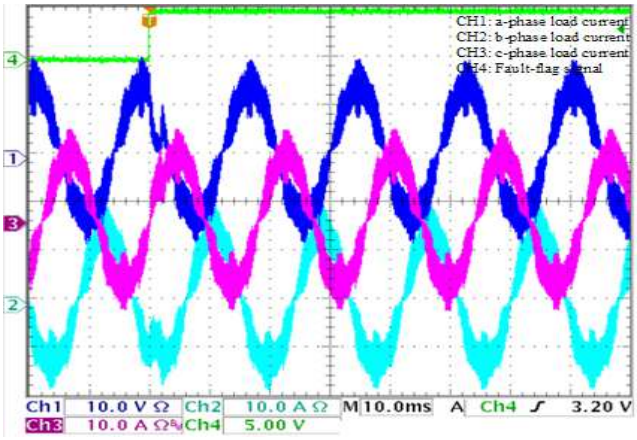


(a)

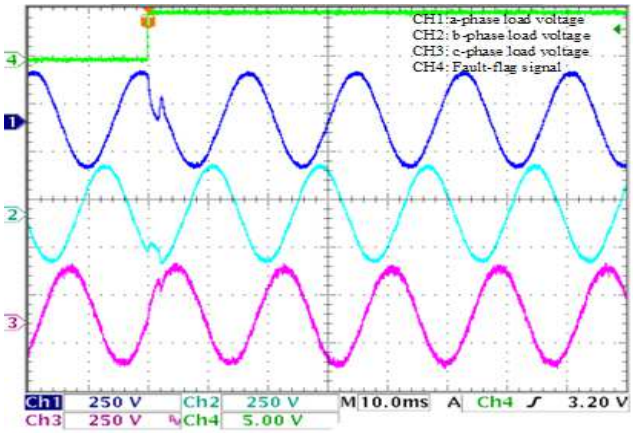


(b)

Fig. 7. Experimental results in case of short-switch fault of S_{ap}: (b) the fault signal, the voltage across the switch S_{an}, the current through the faulted switch S_{ap}, and the load current of the faulted phase; (a) the fault signal and three-phase currents.



(a)



(b)

Fig. 8. Experimental results in case of open-switch fault of S_{ap}: (a) the fault signal and three-phase currents; (b) the fault signal, and the three-phase voltage.

a-phase leg. It can be observed that the system transitions to the post-fault operation that is the same as normal operation after a disturbance of approximate 1.8 ms due to the fault.

VI. Conclusion

A fault-tolerant powertrain for series hybrid electric vehicles has been presented. The newly proposed drive system features nearly disturbance-free operation of the HEVs for open-circuit and short-circuit faults of IGBTs and diodes. Therefore, the vehicle safety has been improved. Moreover, the superior post-fault operating performance allows the vehicle to operate over a sustained long period of time after faults. The full power operation distinguishes the limping-home capability of this solution from the existing art. The excellent reliability of the proposed topology is verified by the quantitative assessment based on Markov reliability model. The mean time to failure as high as twice that of the standard topology greatly reduces unscheduled maintenance, repair time and repair cost, which would offset the initial cost penalty for additional auxiliary devices. In addition, the time domain simulation and experimental results evidently corroborate that the normal operation the system can be resumed after a short disturbance for short-switch and open-switch faults.

References

[1] M. Ehsani, Y. Gao and A. Emadi, Modern electric, hybrid electric and fuel cell vehicles: fundamentals, theory and design, second edition, CRC press, Boca Raton, 2009.

[2] M. A. Masrur, “Penalty for Fuel Economy—System Level Perspectives on the Reliability of Hybrid Electric Vehicles during Normal and Graceful Degradation Operation,” IEEE Syst. J., vol. 2, no. 4, pp. 476–483, Dec. 2008.

[3] O. Wallmark, L. Harnefors, and O. Carlson, “Control algorithms for a fault-tolerant PMSM drive,” IEEE Transactions on Industrial Electronics, vol. 54, no. 4, pp. 1973–1980, Aug. 2007.

[4] T. H. Liu, J. R. Fu, and T. A. Lipo, “A strategy for improving reliability of field-oriented controlled induction motor drives,” IEEE Transactions on Industrial Applications, vol. 29, no. 5, pp. 910–918, Sep./Oct. 1993.

[5] R. L. A. Ribeiro, C. B. Jacobina, E. R. C. da Silva, and A. M. N. Lima, “A fault tolerant induction motor drive system by using a compensation strategy on the PWM–VSI topology,” in Proc. IEEE PESC, 2001, pp. 1191–1196.

[6] J. R. Fu and T. A. Lipo, “Disturbance-free operation of a multiphase current-regulated motor drive with an opened phase,” IEEE Transactions on Industrial Applications, vol. 30, no. 5, pp. 1267–1274, Sep./Oct. 1994.

[7] S. Bolognani, M. Zordan, and M. Zigliotto, “Experimental fault-tolerant control of a PMSM drive,” IEEE Transactions on Industrial Electronics, vol. 47, no. 5, pp. 1134–1141, Oct. 2000.

[8] D. Kastha et al., “Investigation of fault modes of voltage-fed inverter system for induction motor drive,” IEEE Transactions on Industrial Applications, vol. 30, no.4, pp. 426–433, Jul./Aug. 1994.

[9] J. R. Fu and T. A. Lipo, “A strategy to isolate the switching device fault of a current regulated motor drive,” in Conf. Rec. IAS Annu. Meeting, 1993, vol. 2, pp. 1015–1020.

[10] Y. Song, B. Wang, "Analysis and Experimental Verification of a Fault-Tolerant HEV Powertrain," IEEE Transactions on Power Electronics, vol.28, no.12, pp.5854,5864, 2013.

[11] B.A. Welchko, T.A. Lipo, T.M. Jahns, and S.E. Schulz, "Fault tolerant three-phase AC motor drive topologies: a comparison of features, cost, and limitations," IEEE Transactions on Power Electronics, vol.19, no.4, pp.1108,1116, 2004.

[12] Reliability Prediction of Electronic Equipment, Department of Defense, MIL-HDBK-217F, Dec. 1991.

[13] A. Høyland and M. Rausand, System Reliability Theory. New York, NY: John Wiley and Sons, 1994.