HIGH PERFORMANCE VETRONIC ARCHITECTURE EXPLOITING LEADING EDGE HIGH DENSITY ELECTRONICS

Andrew Silveri
General Dynamics Land Systems
38500 Mound Road, Sterling Heights, MI 48310

ABSTRACT

The modern battlefield demands a high degree of electronic capability for both on board processing and off board command and control. The trend for additional electronic systems on board combat vehicles continues to increase at a geometric rate. Battlefield demands and operational scenarios have resulted in a greater need for, advanced sensor technology, increased processing power, greater connectivity and systems interoperability (VICTORY). The integration of these advanced sensors with communications place a large bandwidth and power demand on the vehicle infrastructure. This paper will identify an advanced vehicle electronic architecture enabled by the latest high density processing technologies. An architecture has been developed and is under continued investigation at GDLS. The architecture includes deterministic network technology for spatial and temporal coherence of the sensor data. It provides a mission capability that is crew centric for any function at any crew station. The integrated architecture provides capabilities greater than the sum of the individual subsystems.

INTRODUCTION

The complex future battlefield will require the ability for quick identification of threats in chaotic environments followed by decisive and accurate threat mitigation by lethal force or countermeasure. Integration and synchronization of high bandwidth sensor capabilities into military vehicles is essential to identifying and mitigating the full range of threats. Advances in high density electronics are enabling successful integration of situational understanding on the move and active protection systems in military vehicles. Situational understanding and active protection systems require real time processing and fusion of high bandwidth sensor data in both temporal and spatial domains. The processing and fusion of the sensor data assimilated with radio and external communication information will provide analysis for high confidence decision aides and automation capabilities. The key enabler for integration of these advanced battlefield functions in military vehicles is an advanced electronic architecture featuring high performance embedded computing communicating over high bandwidth backplanes and networks. High performance embedded computing featuring high density electronics combined with interoperability provided by VICTORY open standards and interfaces will reduce the integration burden for these

advanced functions and provide scalability and flexibility for future upgrades. SWaP-C can be greatly reduced through integration of improved performance per watt processor architectures and consolidation of functions into fewer LRUs. High density electronics increase reliability through reduction in vehicle harnesses as more content is integrated on-chip and at the board level and communicated digitally through backplanes and networks. Integration into battlefield networks will be simplified through connection to a network centric vehicle electronic architecture that can scale to match the bandwidth of future radios and communications. Testing can be simplified by having greater data visibility over the network with a single standard network connection. The architecture can be scaled up and down from the low end market to high end market through modularity at the board level and by providing interoperability through network connectivity and low latency bridging devices for legacy systems.

HIGH DENSITY ELECTRONICS

The embedded computing industry is leveraging the latest high density electronic technology from Intel and other companies to provide high performance embedded computing. The increases in performance per watt of high

density electronics is enabling integrated vehicle functions such as radar processing previously only possible in large ground based servers or bulky single function LRUs. The continued trend to increase the number of processing cores integrated onto a single die in multicore processors is enabling embedded performance that rivals the large servers in ground stations. A single multicore processor in a military vehicle can replace all the computing elements from a previous generation providing huge SWaP-C benefits in a scalable processing platform. The latest trends are leading to embedded System on Chip (SoC) technologies which include ARM processor cores integrated into FPGAs and CPUs with integrated GPU technology. The integration of commercial SoC technologies on single board solutions connected together in a VPX based rugged chassis will provide the performance computing required for high bandwidth sensor processing and fusion in real time applications. Active protection systems rely on fusion of multiple high bandwidth sensors including radar and EO/IR to determine if an incoming projectile is a threat and to apply countermeasures to avoid or intercept the threat.
This requires real time processing of the associated high bandwidth sensors, fusion of the sensor data and analysis of the physics of the projectile trajectory. Once the immediate threat is intercepted the physics calculations can be used to determine the source location of the launch platform.
The vehicle electronic architecture described in this paper provides interoperability by leveraging the same high bandwidth sensors and real time processing across multiple modes of operation including active protection systems, situational understanding, supervised autonomy and other advanced survivability and lethality functions.

TENETS OF ARCHITECTURE

General Dynamics Land Systems has developed an advanced high density electronic architecture that is synergistic with VICTORY architecture and standards.

The high density electronic architecture tenets are:
- High Bandwidth Sensor Processing
- Sensor Fusion
- Deterministic Communications
- Rapid Integration Capability – Sensor "Plug and Play"
- Data/Protocol Conversion
- Increased Interoperability
- Flexible, Scalable and Modular
- Optimization of SWaP-C

HIGH BANDWIDTH SENSOR PROCESSING

Situational understanding on the move combined with advanced target identification and tracking functions in ground combat vehicles will give warfighters a huge advantage over adversaries. The successful vehicle integration of these advanced applications requires an electronic architecture that provides capability of real time processing of high bandwidth sensor data including combinations of high resolution EO/IR, radar, LADAR and acoustic sensors. The vehicle electronic architecture design should match and balance the high bandwidth capabilities across processing elements, memory devices, backplanes and networks. This approach prevents bottlenecks in the architecture that could result in undesired latency. FPGAs are optimized for the front end processing of the high bandwidth sensor data at full data rate (GBytes/s) using massively parallel signal processing blocks. The FPGAs handle the raw sensor data and perform the real time sensor processing. The FPGA based sensor processing is matched with general purpose computing that handles the floating point processing for encoding, decoding and transcoding functions and higher precision processing that improves system dynamic range and improves the signal to noise ratio. Additional floating point functions handled by the general purpose computing are physics based calculations and analytics. The general purpose computing for high bandwidth processing often consists of a high end processor such as an Intel i7 gen 3 combined with a NVIDIA GPGPU as shown in figure 1.
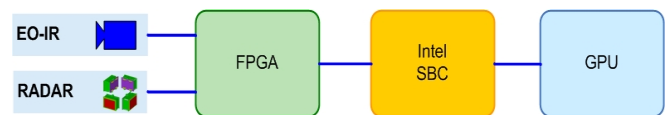

Figure 1: Sensor Processing Architecture

The GPGPU is a massively parallel device that is optimized for processing large chunks of data and performing high rate floating point operations across multiple cores and threads. Current trends in high density electronics will consolidate functionality into fewer chips and boards. The latest generations of FPGAs are system on chip (SoC) devices that have integrated ARM processor cores adding floating point capabilities. The latest 4th generation Intel Core i7 processors include AVX2 for floating point improvements and significant increase in performance of the integrated

GPUs over the previous generation that could eliminate the need for a dedicated GPU as shown in figure 2.

Figure 2: Sensor Processing Architecture with SOC

The high bandwidth data needs to be moved between the processing elements and requires deterministic communication for real time synchronous functions including sensor fusion. One method of synchronizing data across networks depends on time stamping of the data so that it can be aligned at time of receipt. Time stamping of high bandwidth data for sensor fusion applications is not recommended due to processing overhead and increased rate of synchronization errors at high data rates. The key to enabling significant performance advances in high bandwidth processing is realized with direct PCI Express connections over a VPX backplane. The bandwidth provided by 16x PCIe 3.0 provides maximum bandwidth of 32GB/sec enabling high bandwidth and deterministic datapaths across the processing elements and the backplane. In addition to PCI Express the backplanes also have integrated Gigabit Ethernet to support open standard communications. High bandwidth deterministic ethernet network protocols have been developed and it is a matter of time to see which will be widely used in commercial industry with hardware that supports 10GbE and beyond. Deterministic ethernet at 10Gb/s and beyond will provide an increased capability for distributed processing elements for high bandwidth real time functions. Continued popularity of PCI Express in COTS products such as solid state drives will enable scalable bandwidth and modular integration at the card level well into the future. PCI Express interconnects between cards in a VPX based infrastructure enable high performance computing power with reduced SWaP-C.

SENSOR FUSION
Sensor fusion is a technique that combines data from several sensors in order to provide warfighters a comprehensive understanding of the dynamic battlefield environment with a high level of accuracy. Sensor fusion offers the potential for improved situational understanding, active protection, target identification, supervised autonomy and increased analytics capability. The fusion requires real time processing on multiple streams of high bandwidth sensor data. The most efficient way of achieving this requires several types of processors working in parallel linked by high bandwidth deterministic datapaths. FPGAs are optimized for the front end processing of the high bandwidth sensor data in real time and can process multiple sensor inputs in their raw data format and then fuse the raw data. This gives the best fusion results since the data is uncompressed and in its highest resolution format. Sensor fusion can be performed on both onboard vehicle sensors and externally linked sensors from UAVs and battlefield sensors that provide adequate resolution. The high bandwidth processing and fusion performed in the FPGA is enhanced by the Intel microarchitecture providing analytical algorithms and automation functions. The sensor fusion and analytics provide the warfighter with real time situational assessment. The real time sensor data can be fused with non-deterministic battlefield information to provide an even higher level of battlefield assessment to provide coordinated decision aides as shown in figure 3.
There is an abundance of Intellectual Property (IP) cores being developed commercially that can be quickly integrated into the sensor processing and fusion functions. The latest FPGA development environments allow IP from multiple vendors and sources to be combined which allows for rapid integration of the logic from multiple sources. Programming languages such as SystemC allow software coders familiar with C and C++ to program FPGAs. Prior to SystemC programming FPGAs required an expertise in Hardware Description Language (HDL). Developers can also model FPGA logic in Matlab and Simulink and automatically generate verified HDL code for FPGAs. These advances in the FPGA development environment will result in an increase in available commercial IP cores and rapid integration capabilities.
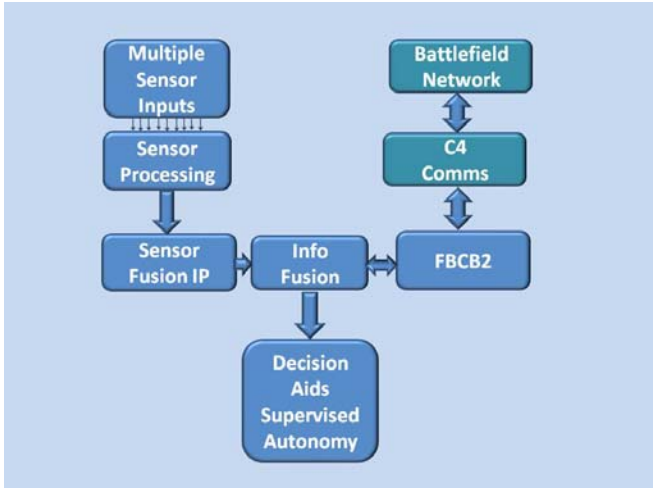
Figure 3: Sensor Fusion combined with Field Data

Figure 4: Sensor Plug and Play

existing and emerging industry standards to any output format for video and display as shown in figure 4. The "plug and play" conversions are optimized for very low latency processing and delivery from sensor to display glass.
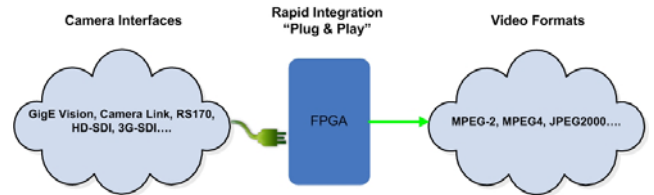
DETERMINISTIC COMMUNICATIONS

The front end FPGA processed sensor data can be sent to other processing elements via PCI Express in architectures with VPX backplanes or sent to separate processing LRUs using deterministic network protocols. VPX supports dedicated high speed serial channels between cards providing high bandwidth data transfers through the backplane. The point-to-point serial links provide both high data throughput and deterministic latency between processing elements. Deterministic Ethernet protocols have emerged such as Time Triggered Ethernet AS6802 and Ethernet Audio Video Bridging (AVB). These protocols are currently being evaluated with the Time Triggered Ethernet having an early edge for mission critical applications discussed in this paper. Deterministic Ethernet networks and PCI Express through the VPX backplane provide for high bandwidth deterministic communication between LRUs and VPX cards respectively. This is required for synergy and interoperability between mission critical functions such as fire control and hit avoidance. It is also an optimal solution for automation of mission critical and safety critical functions.

RAPID INTEGRATION CAPABILITY – SENSOR "PLUG AND PLAY"

The front end FPGA processing can provide rapid integration of sensors with integrated IP cores that will process sensor input data in any format from a large group of

DATA/PROTOCOL CONVERSION

Standardization of interfaces and data formats needed in open standard architectures such as VICTORY will require data/protocol conversions from legacy systems and tightly controlled real time mission critical functions. The data conversion rates can be prioritized based off different levels of criticality in the vehicle systems. The data from high bandwidth sensors has already been addressed in the "High Bandwidth Sensor Fusion" section of this paper. Powertrain, power management, and inertial data can come from multiple LRU sources and is usually resident on deterministic networks including CAN and 1553. Data that is continuous in nature such as from gyro sensors will need to be converted at higher data rates than discrete data to be useful for interoperable dynamic functions that reside on multiple LRUs. Ethernet is the network of choice for most open standard architectures including VICTORY. Network bridges are required to convert data between the legacy protocols (1553, CAN and other network protocols) to Ethernet. The processing load for these types of data/protocol conversions can cause bottlenecks in the data distribution if not addressed properly. The parallel signal processing blocks in FPGAs are ideal for these types of data/protocol conversions. Updates to data formats in the vehicle can be accommodated quickly in the FPGAs due to their reconfigurable logic.

INCREASED INTEROPERABILTY

Interoperability that enables data exchange and functional sharing between processing functions from distributed processing elements with different communication protocols will enable rapid integration of new hardware and software technology at lower costs and facilitate more effective fire control, survivability, mobility and automation functions. Interoperability across previously "stovepiped" subsystems will provide capabilities greater than the sum of the individual subsystems. The vehicle integration of high bandwidth sensors such as radar for an active protection system should be applicable to all systems based off priorities of the operating modes. The radar could also be utilized by fire control and automated operation functions within the vehicle platforms. Many legacy systems have single function sensors and displays. The architecture shown in figure 5 would enable multi-function displays that process any input and convert to any output for distribution to any display or processing element. The commander of the vehicle can quickly configure a screen to see any sensor data and related analytics that will greatly benefit the situational assessment. The screen content could be sent to any other display in the vehicle to disseminate information to the rest of the crew. The access control is handled in the multi-core CPU to keep information accessible within the user's allowed clearance level. The screens become a means of communicating with other crew members through use of graphics and information for quick situational understanding. The presentation of sensor data and sensor fusion can be optimized with analytics and decision aides that would lessen the cognitive load on the crew.
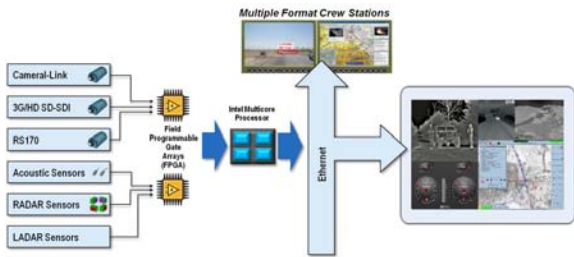

Figure 5: Process any Input – Convert to any Output

FLEXIBLE, SCALABLE AND MODULAR ELECTRONIC ARCHITECTURE

Exponential growth in electronics capabilities make it difficult to keep up with increasing rate of obsolescence. This combined with the need to add more processing power and I/O expansion with incremental changes require a

flexible and scalable electronic architecture as shown in figure 6. A modular chassis that supports upgrades at the processor board level as opposed to whole LRU replacements is more efficient. The chassis can also have a removable backplane that can be quickly upgraded to next generation communications that support higher bandwidth protocols to meet increased functionality. A system with modular LRM chassis can be quickly upgraded at the card level with minimal impact on the architecture. The modular electronic architecture provides flexibility for multiple combinations of processing elements for different platforms and can be scaled up or down by replacing or removing boards.
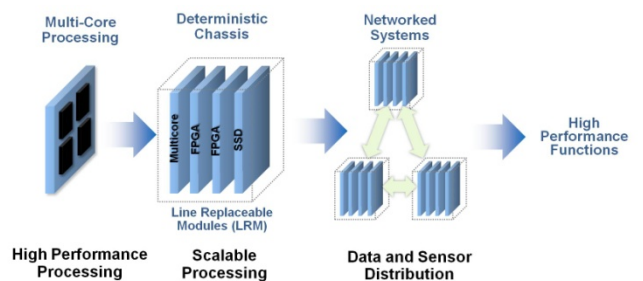

Figure 6: Scalable Infrastructure

OPTIMIZATION OF SWaP-C

Performance gains from high density electronics can be used to reduce SWaP-C and increase reliability. The combination of multi-core processors and a VPX chassis reduces the LRU related SWaP-C by reducing the number of LRUs and associated processors. The stand-alone processing units are consolidated into a single board multi-core processor in a LRM as shown in figure 7. An advanced multi-core processor is used to consolidate the processing that was previously distributed amongst five Abrams LRUs including the Driver Information Display (DID), Commanders Electronic Unit (CEU), Gunners Control Display Panel (GCDP), Mission Processing Unit (MPU), and FBCB2 unit (Force Battle Command Brigade and Below). The multicore processor has four processor cores on a single chip mounted on a 3U VPX board. Each core on the multicore processor can host the functions previously hosted on individual single board computers. The LRU consolidation reduced the processing power consumption by a factor of eight and

reduced the weight and size footprint by a factor of four. Reliability is greatly increased due to the significant reduction in harness interconnects as a result of the LRU reduction.
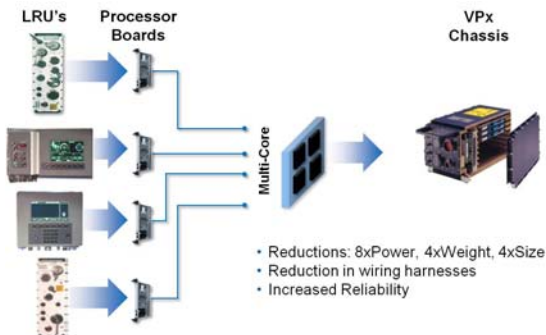

Figure 7: SWaP-C Reduction

REFERENCE ARCHITECTURES

Vehicle Electronics reference architecture with distribution of computing resources over a network.

Figure 8: Highly Distributed Architecture

Vehicle Electronics reference architecture with distribution of computing resources through a modular backplane and over a network.
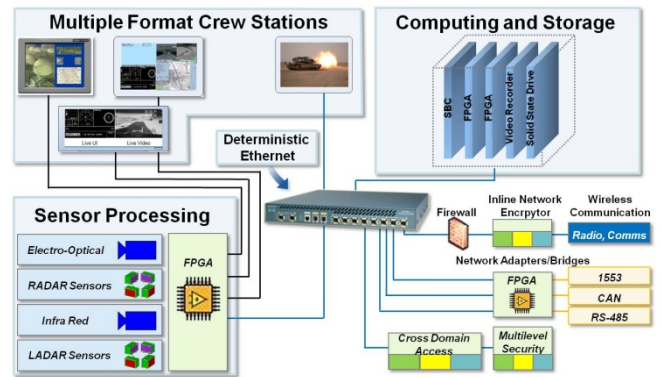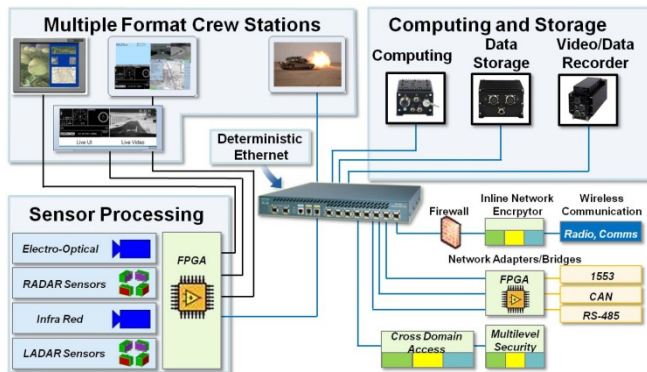

Figure 9: Distributed and Modular Architecture

CONCLUSION

The vehicle electronics architecture under development at General Dynamics Land Systems provides for rapid integration of high performance functions with the benefit of greater network connectivity and system interoperability. The electronic architecture is optimized for functional scalability to enable future growth including integration of advanced sensor technology providing our warfighters with the advantages of situational understanding and active protection systems. The low latency data and protocol conversion technology provide the means to integrate both new and legacy components that are compliant to VICTORY architecture standards and interface specifications. Modernization and incremental updates can be easily and affordably managed well into the future without any major infrastructure changes.