

Open Standard Approach for Parallel Development of High Performance C4ISR/EW Capabilities for Ground Vehicles

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ABSTRACT

Ground Combat Vehicles mission requirements challenge the Military and Aerospace community to provide the right amount of electronics into constrained size, weight, power and cost (SWaP-C) for any given capability. The military system integrator has to balance the physical, thermal and electrical constraints of the vehicle against the vast amount of compute power required to provide signal processing for C4ISR/EW applications. Due to processor silicon limitations, system integrators typically develop optimized proprietary box-level systems. The issue is that Moore's Law and changes in mission can make these single-use systems already obsolete by the time they are finally adopted by the armed forces. Curtiss-Wright's experience in open standard-based High Performance Embedded Computing (HPEC) provides a unique perspective for the use of open architecture scalable signal processing for highly SWaP-C constrained Military Vehicles. The open standard approach allows for well-managed and planned technology refresh that mitigates obsolescence, and provides the system integrator with parallel paths of software and hardware development to successfully meet the fielding milestones.

INTRODUCTION

The paper will illustrate the parallel development paths for software and hardware for Ground Combat Vehicle (GCV) C4ISR/EW processing systems. It will show the historical and expected gains in hardware performance across technology refresh cycles and the SWaP-C reduction over time for a fixed amount of processing capacity.

Examples of HPEC C4ISR/EW systems and their different types of processing capability will be provided and compared to potential SWaP-C optimized processing capabilities of tomorrow's ground vehicles. This will provide the audience with an understanding of potential new C4ISR/EW capabilities now possible for the ground vehicle environment. A discussion of how an open standard approach for GCV systems, that leverages low-risk parallel development paths, will highlight how the technology refresh of processing hardware will meet the evolved C4ISR/EW capability requirements at the time of fielding.

THE PROBLEM

The amount of electronics required to protect and facilitate the GCV mission has exponentially increased as the threat continues to evolve and adapt to current Military capability (Figure 1). Ultimately, a key limit for all GCVs that require the increasing amounts of compute resources to support the various C4ISR capabilities desired is determined by the amount of fuel that the vehicle can carry. An unsustainable problem is presented by today's "stovepipe" approach to equipment deployment, which unavoidably creates significant amounts of electronic redundancy. As GCVs are tasked to support more and more equipment, they are becoming overburdened; even to the extent of causing, the vehicle wheels to "splay" outward (figure 2). For GCVs to enable support of their C4ISR missions, this stovepipe approach for electronic equipment has to end.

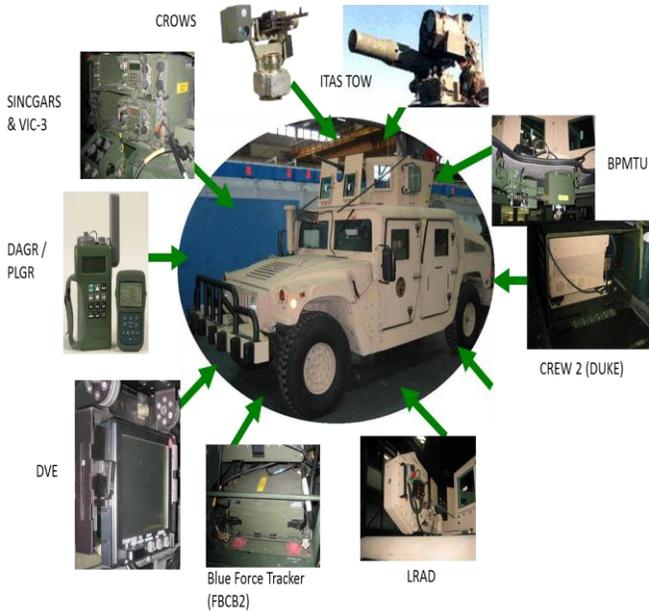


Figure 1: GCV Electronics electronic sub-systems.



Figure 2: Splayed tires on an overburdened GCV.

THE POSSIBLE SOLUTION

When one breaks down C4ISR solutions into their individual functions, one finds a strong and striking similarity amongst them. At a basic level, every type of C4ISR electronic system, from RADAR, Communications, SIG-INT and Command and Control, comprises five basic functions or sub-systems. These five functions are Acquire, Digitize, digital signal processing (DSP), Store and Human Machine Interface (HMI) (figure 3). The Acquire function converts analog real world data into a digital-ready form. This function ranges from a completely integrated smart sensor, such as an electro optical signal pod that converts analog data directly into network data packets, or

tuner systems that down/up convert radio frequency to/from lower frequency bands, to a simple engine temperature controller on the engine block. The Digitization sub-system converts the analog signal, then filters, formats, and pre-processes the digitized data for the DSP sub-systems. The DSP function hosts the algorithms and processing capability that reduce the digitized data to actionable functions, which can be stored or provided to the HMI, or in some systems, convert the processed data back to analog and send it out as a signal to the real world.

System integrators can combine all five of these basic functions onto one circuit board, or separate them into multiple individual components connected by high-speed networks or backplanes. One approach for separating the components is to develop specialized cards optimized to that specific function. Unfortunately, integrators often repeat these basic five functions for every individual electronic system in the GCV, which exacerbates the vehicle's electronics system SWAP-C equation.

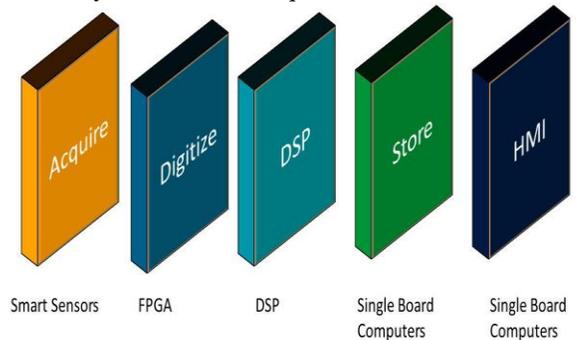


Figure 3: Five functions of C4/ISR solutions.

C4ISR solutions examples

The following examples of C4ISR sub-systems represent real world design proposals for current military customers.

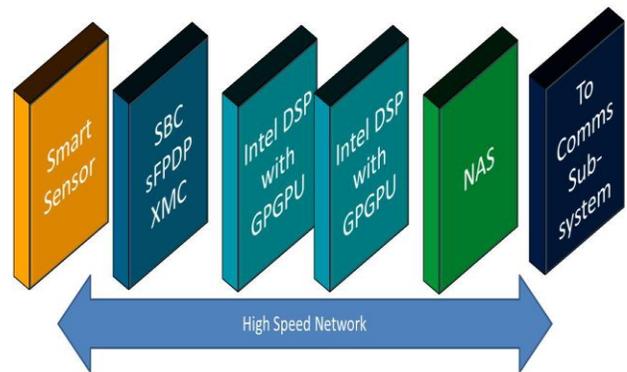


Figure 4: SAR RADAR system.

Example 1: RADAR (SAR and Target Recognition)

The SAR and Target Recognition RADAR system (figure 4) connects with a SAR sensor that brings in data using the high-speed sFPDP data protocol. This data is converted to a standard data network and sent to a DSP sub-system that processes the image, which can be stored or sent to a communications system. The communications sub-system sends the data to an analyst via a wireless network.

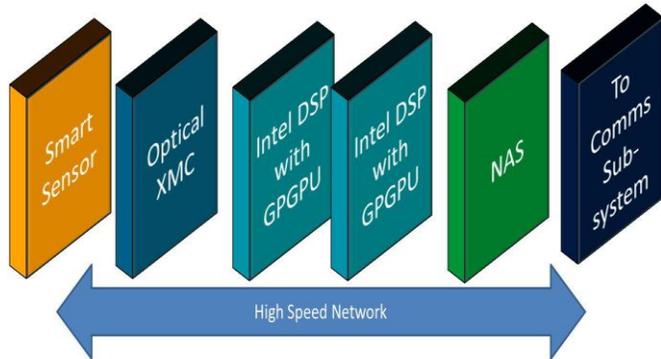


Figure 5: Situational Awareness

Example 2: Situational Awareness

The situational awareness (SA) system is very similar to the RADAR system, but it connects to an electro-optical sensor. In the SA system, the image data is collected, compressed, and forwarded to a storage system or to an analyst who is connected wirelessly via the communications sub-system.

Example 3: SIG-INT

The next example (figure 6) is a SIG-INT sub-system. A key difference between the SIG-INT system and the SAR and SA systems is that its acquire function is a digital down convertor. The purpose of a SIG-INT is to acquire RF signals, and then filter, and identify signals of interest for use by analysts. The analyst could be a vehicle-based operator or the signals could be transmitted wirelessly to a remote analyst located far from the vehicle.

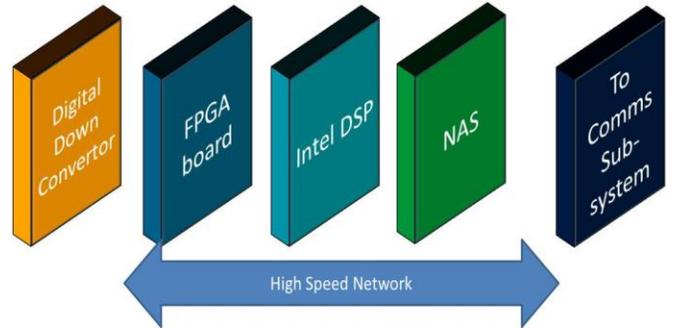


Figure 6: SIG-INT

Example 4: Communications

Our last example is the Communications (COMS) sub-system. While similar to the SIG-INT sub-system, the COMS sub-system adds a digital up-convertor component. COMS and SIG-INT systems receive signals in similar fashion, but the COMS sub-system has the ability to transmit data to the wireless network via its digital up-convertor (figure 7).

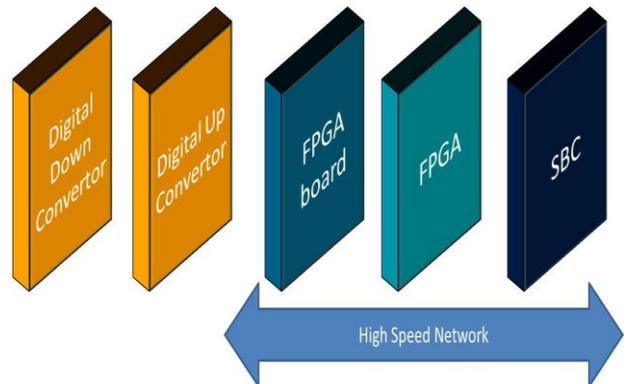


Figure 7: Communications Sub-system

The "god-box"

One approach for eliminating the electronics component redundancy currently found on GCVs, and thereby significantly reduce SWaP-C, is to enable the system integrator to combine all the sub-system function types into a single chassis, providing a single platform that combines, and supports all types of C4ISR missions into one platform. An example of this approach, which we here refer to as a "god box," is shown below (figure 8).

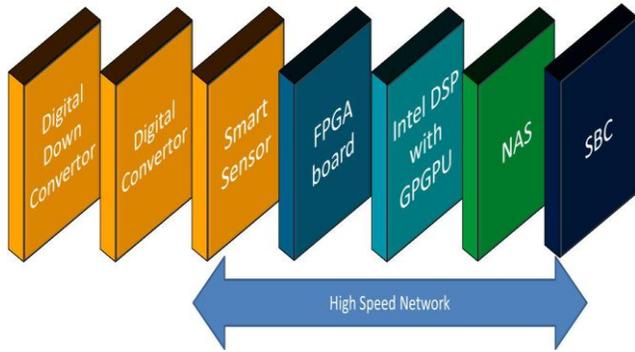


Figure 8: The “god-box”

The “god box” approach enables a system integrator to optimize their processing solution to meet their largest mission requirement while further optimizing the platform for size, weight and power. In response to changes in mission requirements, the “god box” provides the flexibility needed to support different algorithms, which can be adapted dynamically to use more or fewer resources. This dynamic adaptation would enable the integrator to modify power consumption and extend mission range as desired. Key to the success of the “god box” concept is an external network or backplane able to support the bandwidth requirements of the platform sensors. Today, the five basic C4ISR functions that we’ve described do not typically use a common network, processor, or form-factor. Today’s lack of commonality makes it impractical for the platform integrator to combine these functions into a single box using common software. This is because the development of universal interface standards and software middlewares tools is still very immature for GCVs, and in fact, for the military in general. In addition, industry and military consortiums such as ROSA (RADAR) and Iron Symphony (SIG-INT) have not yet defined how each of these standards can be combined together. The U.S. Army’s VICTORY standard attempts to define how disparate systems can communicate together, but the next step of defining a standard interface for the five basic C4ISR electronic sub-system functions have yet to be defined.

COTS Solutions

COTS provides a solution today. In recent years, COTS solution providers have worked diligently to provide the requisite components to build a “god-box.” Working with standards bodies such as the VITA Standards Organization (VSO), COTS providers have defined a new form-factor, the communications planes that enable standardized backplanes, and a variety of rugged modules and systems based on these standards. These COTS standards provide the basis of interoperability, enabling system integrators to upgrade a

system’s modules as technology improves. The latest COTS standard for deployed C4ISR systems is OpenVPX™/VPX (VITA 65/46). This standard is the COTS industries answer to the scalable electronics for GCVs.

VPX leverages the popular Eurocard 3U and 6U form-factors. Defense and Aerospace system integrators have used modules based on these form-factors, such as VME and CompactPCI boards, in rugged embedded applications for many years. Similarly, the new VPX module standard has provisions for support of the industry de facto I/O mezzanine module standards, PMC and XMC, but also adds a P0 connector for power, reference clocks, geographical pin assignments, JTAG, non-volatile write protection, system reset and out-of-band management. In addition, the VPX standard also specifies a new connector that supports the latest serial fabric technology, special alignment posts, card keying, safety grounds, and 160 (3U) or 480 (6U) signal connections. A variant of VPX, VPX-REDI (VITA 48), defines module ESD covers, larger horizontal pitch widths to accommodate the latest high-performance silicon, as well as support for the broad range of cooling methodologies.

The key differentiator of the VPX form-factor is its new connector, the Multi-Gig RT2. This wafer-based connector provides special ESD ground planes, single-ended connections for bussed type signals, and differential paired (diff-pair) traces specifically designed to route high-speed SERDES type communications between modules on a backplane. The connector vendor, Tyco, has designed the Multi-Gig RT2 connector to support signal speeds up to 10-Gigahertz, which accommodates USB 2.0, PCIe™ 2.0, RapidIO™ 2.1, 10/40GigE, FPGA SERDES and other high-speed serial fabrics.

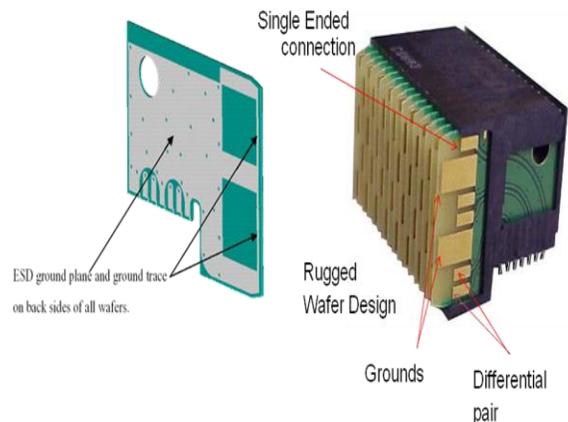


Figure 9: Multi-Gig RT2 wafer and connector

Additional VITA standards such as VITA 60 and VITA 63 provide definition of alternative connectors that could replace the Multi-Gig connector for even more vibration and

shock intense applications. Other new VITA standards define connectors for special signal capabilities such as optical (VITA 66) and radio frequency (VITA 67). The VPX™, VPX-REDI™ and other related VITA specifications have been written to support the current and future processing and data-communication technologies for the MIL/Aero market.

VPX - the issue

Regardless of the connector strategy used, the problem with the serial fabrics in today’s C4ISR systems is that they employ point-to-point connectivity. Therefore, when defining the backplane for two or more VPX modules with serial fabrics, the system designer must connect each diff-pair to exactly one other module’s diff-pair. Most serial fabrics are based on duplex communications so that one lane requires four connection pins (one module’s diff-pair transmits to another module’s diff-pair receive port, and vice versa).

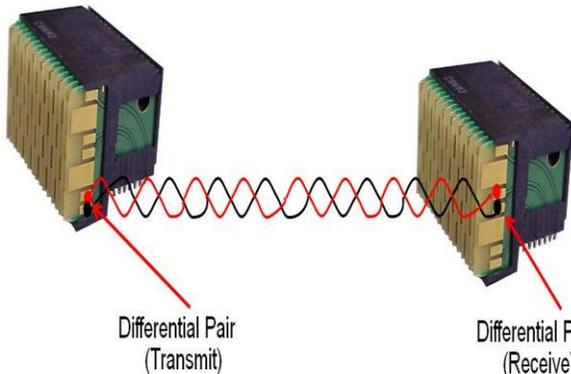
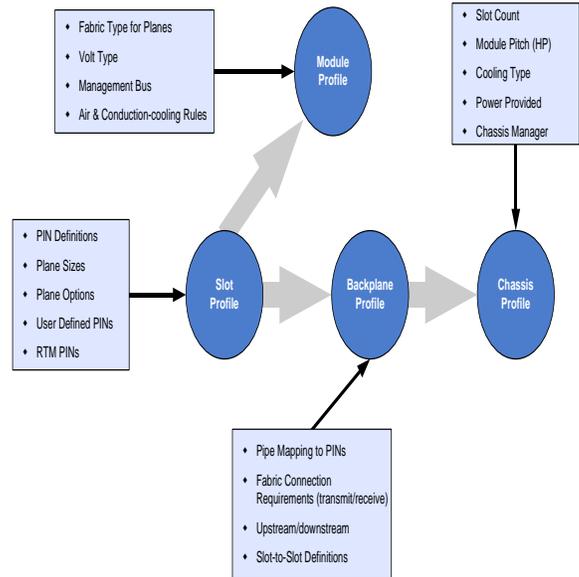


Figure 10: SERDES connection between two Multi-Gig RT2s

As more VPX modules are added to a system, more connection pins become necessary for data communications. Designers can aggregate the diff-pairs together for larger data bandwidth, but this takes an even greater number of connections. Even with 480 (for 6U) or 160 (for 3U) pins available to the VPX module designer, enabling high-bandwidth serial communications connectivity between numerous modules t can quickly utilize most of the available pins, leaving very few free for specialized module I/O.

The OpenVPX™ standard defines four profile types: slot, module, backplane and chassis. Because interoperability starts at the module level, the fundamental profile is the slot profile. The slot profile provides basic definitions for planes (type, number, and size) and user-defined pins. A backplane profile defines how the slot profiles are connected. Chassis profiles add mechanical specifications, input power, and slot

number to guide in specifying the appropriate chassis. Lastly, the module profile defines how module vendors apply specific fabrics to the slot profiles. The module profile also provides definitions of fundamental module characteristics. Using these four OpenVPX™ profiles, system integrators can easily integrate different VPX™ vendor modules, backplanes, and chassis into a system.



Fundamental to this system approach is the definition of pin connections are. In OpenVPX™, a “pipe” comprises connections made up of diff-pairs. For example, an Ultra-Thin Pipe (UTP) is two (2) diff-pairs or four (4) connections on a VPX Multi-Gig connector. A Thin-Pipe (TP) is four (4) diff-pairs and a Fat-Pipe (FP) is eight (8) diff-pairs. Fat-Pipe grouping expands to Double Fat Pipe (DFP), Quad Fat Pipe (QFP), and Octal Fat Pipe (OFP) to describe the largest bandwidth plane needed.

The “plane” is the type of communication that uses pipes. For example, based on the profile definition, if a plane has 1.0 Generation PciExpress fabric on an UTP this would equal one lane (x1) of PciExpress at 2.5 Gigabits per second duplex. Alternatively, using Ethernet, UTP could be 1000BaseBX, TP would be 1000BaseT, and a FP would be 10GBase-K4 or XAUI. In OpenVPX™ planes are defined as interoperable data connections between modules.

	Ultra Thin (UTP)	Thin (TP)	Fat (FP)	Double Fat (DFP)	Quad Fat (QFP)	Octa Fat
Lane	1	2	4	8	16	32
Diff-pairs	2	4	8	16	32	64
Connections/Pins	4	8	16	32	64	128
Ethernet	1000 Base-Bx	1000 Base-T	10G Base-K4 (XAUI)	Two 10GBase		
PCIe	x1	x2	x4	x8	x16	x32
PCIe Gen 1	2.5 Gb/s	5 Gb/s	10 Gb/s	20 Gb/s	40 Gb/s	80 Gb/s
PCIe Gen 2	5 Gb/s	10 Gb/s	20 Gb/s	40 Gb/s	80 Gb/s	160 Gb/s

Table 1: Pipe Definitions

Planes and User I/O

OpenVPX™ also makes a distinction between planes and user-defined pins. Planes are wafer pins routed through the backplane to other wafer pins. For example, if a backplane topology calls for one (1) fat pipe routed to another slot, then that connection pipe is a plane (see Table 1). User-defined wafer pins connect through the backplane to a rear-transition module (RTM). There is no slot-to-slot connection of these pins. The VPX module developer could use these user-defined pins for any purpose without worrying about interoperability with other modules. Fabric connections that are not part of a plane have no connection to another slot or to the RTM. With this type of system-level specification, OpenVPX™ defines interoperability at the mechanical, module, and the backplane level.

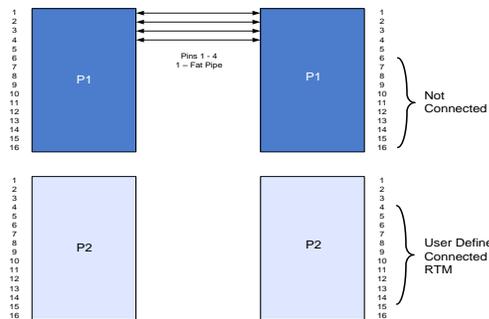


Figure 11: Simple 3U Two-Slot Example

For example, a simple two-slot backplane is able to connect two boards with one DFP interconnect (see Figure 11). A three-slot backplane can connect three VPX modules with Slot 1's FP

A connected to Slot 2's FP A, and Slot 1's FP B connected to Slot 3's FP A (see Figure 12).

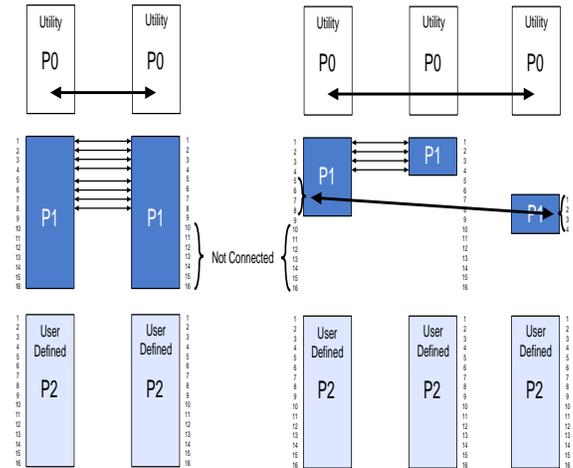


Figure 12: Simple 3U 2-Slot and 3-Slot Example

One type of OpenVPX™ backplane profile is the 6U 16-slot backplane, which is shown in Figure 13.

This 6U 16-slot profile exemplifies the expansion plane. Also shown (Fig. 13) is the utility plane, which contains a set of power, ground, and utility signals bussed between all of the slots. The control plane is where user applications would coordinate utility plane information between blades for reliability, availability, and serviceability functions. The data plane comprises the typical high-bandwidth, low latency pipes that are specified for large data movements at a system level. Depending on which profile is specified, each one of these planes can be optimized for application requirements.

Many electronic systems require low-latency high-bandwidth connections at the data plane. Meshed and centrally switched architectures each have corresponding advantages and disadvantages, depending on what function will be instantiated by which COTS boards. By simply changing system software, different algorithms can take advantage of the different backplane connections. Serial data streaming connections can use the expansion bus such that data can flow from board to board without using the central switch. If the system needs a more distributed system like a data broadcast, then one node could broadcast to every other board in the system using the central switch. The central broadcast could be a low data rate signal using Ethernet on the control plane or a Serial RapidIO™ broadcast on the data plane. Of these capabilities, requires either different hardware or backplane configuration. They only require a simple change of software.

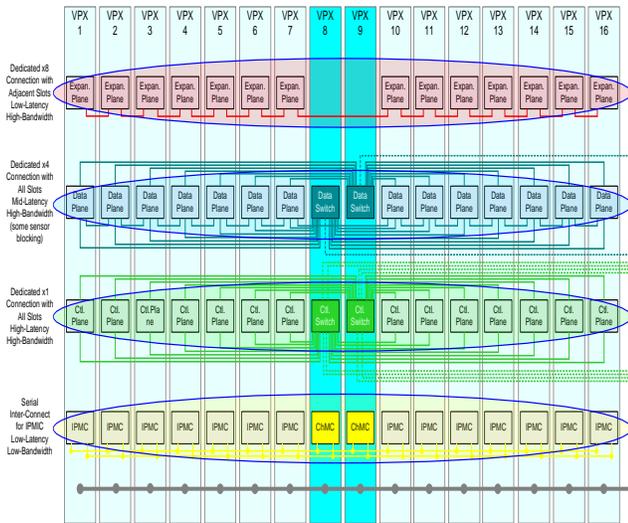


Figure 13: 6U 16 Slot backplane

As capability needs change in response to changes in the mission, system integrators can add more blades into the system to add processing power or redundancy. In addition, next generation DSP systems can be added into this architecture as new technology becomes available.

THE FUTURE

Some DARPA/Research Lab programs are striving to improve SWaP-C for some military platforms. These programs are essentially first steps towards the god box concept that integrate two or more C4ISR functions into one large integrated system connected by a universal network. For example, the ACT program, is attempting to create a

scalable array that can act as a RADAR or Communications system that "... may save billions of dollars" and prevent the DoD from developing a new array from scratch [1]. The program will also adapt "... that array so that it can communicate with each other to function as a single large array. [1]" This will combine the communications and RADAR systems and would allow the same ISR box to control the RADAR and the communications function of the array. In another example, the FLEXDAR, program being developed by the Office of Naval Research (ONR) will combine Communications and RADAR systems to "increase detection and firm-track range, improve electronic protection, improve tracking ..., improve detection of targets in clutter, support operation during emissions control, use of aperture to transmit/receive network data and improve availability [2]."

These programs are proving that Communications and RADAR functions can be combined into a single system, and that ability to add SIG-INT, Electronic Attack and Protection will soon follow. We can now provide system integrators with the ability to control and improve their C4ISR system functionality while making it easier for them to leverage the latest technology on Military platforms. With the addition of the latest open standards, middleware and module level interoperability, the goal of SWaP-C-efficient GCV electronics is fast becoming a reality.

REFERENCES

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