2014 NDIA GROUND VEHICLE SYSTEMS ENGINEERING AND TECHNOLOGY SYMPOSIUM
VEHICLE ELECTRONICS AND ARCHITECTURE (VEA) TECHNICAL SESSION
AUGUST 12-14, 2014 – NOVI, MICHIGAN

VEHICLE ELECTRONIC ARCHITECTURE FEATURING DATA MANAGEMENT FOR REAL TIME SENSOR DRIVEN CAPABILITIES

Andrew Silveri
General Dynamics Land Systems
38500 Mound Road, Sterling Heights, MI 48310

ABSTRACT

The complex future battlefield will require the ability for quick identification of threats in chaotic environments followed by decisive and accurate threat mitigation by lethal force or countermeasure. Integration and synchronization of high bandwidth sensor capabilities into military vehicles is essential to identifying and mitigating the full range of threats. High bandwidth sensors including Radar, Lidar, and electro-optical sensors provide real-time information for active protection systems, advanced lethality capabilities, situational understanding and automation. The raw sensor data from Radar systems can exceed 10 gigabytes per second and high definition video is currently at 4 gigabytes per second with increased resolution standards emerging. The processing and memory management of the real time sensor data assimilated with terrain maps and external communication information requires a high performance electronic architecture with integrated data management. GDLS has developed an advanced modular architecture that features high performance embedded computing communicating over high bandwidth backplanes and networks that enables the integration of advanced applications utilizing high bandwidth sensors. A high level description of the architecture with a focus on memory design and management will be provided.

INTRODUCTION

Advances in high density electronics are enabling successful integration of high bandwidth sensors to detect, recognize and identify targets and threats. Real time processing of the sensor data is essential for situational understanding on the move, active protection systems, and electronic warfare in military vehicles. Situational understanding and active protection systems require real time processing and fusion of high bandwidth sensor data in both temporal and spatial domains. Active protection systems rely on multiple high bandwidth sensors including radar and EO/IR to determine if an incoming projectile is a threat and to apply countermeasures to avoid or intercept the threat.

Real time processing and fusion of the sensor data is critical for detection and countermeasure capability for active protection systems and intelligent fire control. The key enabler for integration of these advanced battlefield functions in military vehicles is an advanced electronic architecture featuring high performance embedded computing communicating over high bandwidth backplanes and networks. The high performance architecture provides situational understanding on the move to the vehicle crew and enables the vehicle to act as a node on the battlefield network sharing real time sensor data with ground soldiers and mobile command centers. Situational understanding and active protection systems require real time processing and fusion of high bandwidth sensor data in both temporal and spatial domains. Management of the sensor data is critical both at the micro level in memory and at the subsystem application level. General Dynamics Land Systems has developed an advanced modular architecture featuring high performance embedded computing paired with sensor data resource management. In addition to high performance sensor processing capabilities the modular architecture was designed for interoperability and provides the foundation for VICTORY open standards and interfaces. The flexible architecture will reduce the integration burden of emerging high bandwidth sensor based functions and provide scalability and flexibility for future upgrades. SWaP-C is significantly reduced through integration of improved performance per watt processor architectures and consolidation of functions into fewer LRUs. Reliability is increased through reduction in vehicle harnesses as more content is integrated on-chip and at the board level and communicated digitally through backplanes and networks. Integration into battlefield networks will be simplified through connection to a network centric vehicle electronic architecture that can scale to match the bandwidth of future radios and communications. The architecture can be scaled up and down from the low end market to high end market through modularity at the board level and by providing interoperability through network connectivity and low latency bridging devices for legacy systems.

HIGH BANDWIDTH SENSOR PROCESSING

The advanced modular electronic architecture developed at GDLS featuring high performance embedded computing provides a real time computing infrastructure for interoperable high bandwidth sensor driven applications including sigint, ISR, electronic warfare, situational understanding, active protection systems, autonomy, and advanced lethality capabilities. The modular architecture features an optimal combination of FPGA, Multicore CPU and GPU processors linked together with PCI Express Gen 3 (PCIe 3.0) in an Open VPX chassis as shown in figure 1. The architecture supports high bandwidth sensor integration and fusion by delivering up to 32 gigabytes per second data flows between the processing elements. In addition to the high bandwidth data transfers the PCIe 3.0 interface provides deterministic system response and low latency communication for real time synchronous functions including sensor fusion. The FPGA performs front end processing of the high bandwidth sensor data at full data rate (GBytes/s) using massively parallel signal processing blocks. The FPGA handles the raw sensor data and performs the real time sensor processing. The FPGA based sensor processing is matched with general purpose computing that handles the floating point processing for encoding, decoding and transcoding functions and higher precision processing that improves system dynamic range and improves the signal to noise ratio. Additional floating point functions handled by the general purpose computing are physics based calculations and analytics. The general purpose computing for high bandwidth processing often consists of a high end processor such as an Intel i7 gen 3 combined with a NVIDIA GPU. The GPU is a massively parallel device that is optimized for processing large chunks of data and performing high rate floating point operations across multiple cores and threads.

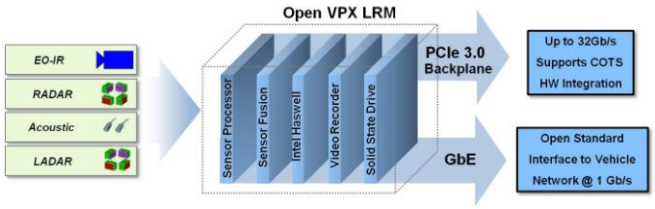

Figure 1: Sensor Processing Architecture

BALANCED ARCHITECTURE

Vehicle electronic architecture designs should strive to result in a balanced system. The high bandwidth capabilities across processing elements, memory devices, backplanes and networks should be matched as close as possible. This approach reduces bottlenecks in the architecture that result in undesired latency. CPU performance should closely match interconnect bandwidth in order to take advantage of sensor data and eliminate any potential data-processing bottlenecks. Functional partitioning between the FPGA, CPU and GPU should be designed to take advantage of their unique processing architecture. The layout of data structures used by the algorithms, their location and movement between memory is another key to a balanced approach. System response and data latency can be significantly reduced through taking advantage of the growing amount of processor parallelism that is designed into these devices. The data handling and flow is critical in real time systems.

DATA AND RESOURCE MANAGEMENT

Management of data and resources in the high performance embedded computing architecture will increase throughput performance and reduce latency significantly. In legacy computing systems exchange of data between CPU main memory and other processing elements or I/O devices required full CPU utilization for the entire duration of the read or write operation resulting in congestion on the bus leading to latency issues. Standard features in PCI Express enhance data sharing between connected devices. Direct Memory Access (DMA) is a technique used for efficient transfer of data to and from host CPU system memory. The CPU only initiates the transfer and then is fully available to perform other operations resulting in better overall system performance. DMA transfers between the FPGA and CPU frees the host processor to perform other calculations during data transfer as shown in figure 2. Transferring radar waveform data between the FPGA target and the host can be done in large burst data transfers. The CPU can offload data into host memory that can quickly be transferred for highly efficient processing in FPGA and GPU.

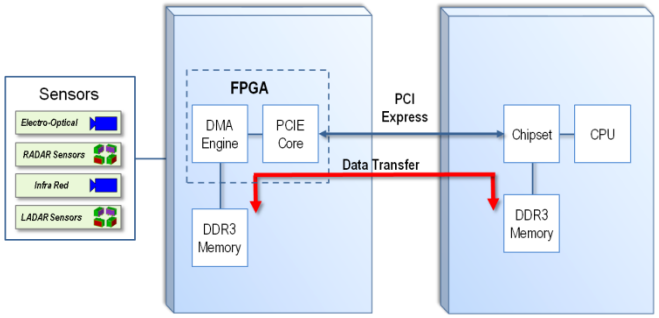

Figure 2: DMA Data Transfer

PCI Express peer to peer (**P2P**) communication specification enables point-to-point transfers between multiple processing elements and I/O devices without sending data through the host processor or memory. Peer to peer communication significantly increases data throughput and further reduces latency. Radar processing in combat vehicles can be achieved by bypassing the CPU and streaming the high bandwidth sensor data from the front end FPGA directly into a back end GPU taking full advantage of the massively parallel processing capabilities. Figure 3 shows the data transfer between FPGA and GPU without P2P and figure 4 shows the data transfer with P2P.

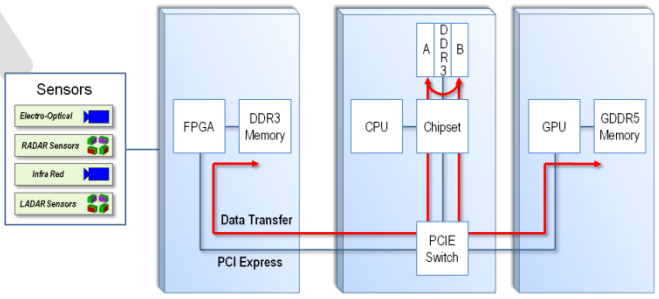

Figure 3: DMA Data Transfer between FPGA and GPU

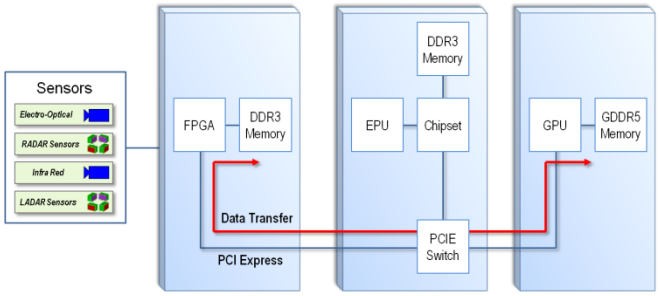

Figure 4: Peer to Peer Data Transfer between FPGA and GPU

PCI Express P2P connections to Solid State Drive (SSD) can significantly decrease access latency and management of persistent data storage. P2P connected SSDs have the advantage of having internal RAID/aggregation of multiple SSDS which would normally need to be performed by the host CPU. SSDS in multiple VPX cards can be aggregated through PCIe connections for additional capacity and performance. The PCI Express connected SSD can also be configured for streaming recording and playback.

SENSOR MANAGEMENT

Sensor configuration and management is performed by the FPGAs. The design objective is to provide multi-mode use for different mission scenarios. The FPGAs can support partial dynamic reconfiguration in which part of the FPGA is loaded with a new logic while the rest of the FPGA is functional. The sensor calibrations can be adjusted on the fly to support changing from a target detection mode to an active protection mode.

SENSOR FUSION

Sensor fusion is a technique that combines data from several sensors in order to provide warfighters a comprehensive understanding of the dynamic battlefield environment with a high level of accuracy. Sensor fusion offers the potential for improved situational understanding, active protection, target identification, supervised autonomy and increased analytics capability. The fusion requires real time processing on multiple streams of high bandwidth sensor data. The most efficient way of achieving this requires several types of processors working in parallel linked by high bandwidth deterministic datapaths. FPGAs are optimized for the front end processing of the high bandwidth sensor data in real time and can process multiple sensor inputs in their raw data format and then fuse the raw data. This gives the best fusion results since the data is uncompressed and in its highest resolution format. Sensor fusion can be performed on both onboard vehicle sensors and externally linked sensors from UAVs and battlefield sensors that provide adequate resolution. The high bandwidth processing and fusion performed in the FPGA is enhanced by the Intel microarchitecture providing analytical algorithms and automation functions. The sensor fusion and analytics provide the warfighter with real time situational assessment. The real time sensor data can be fused with non-deterministic battlefield information to provide an even higher level of battlefield assessment as shown in figure 4.

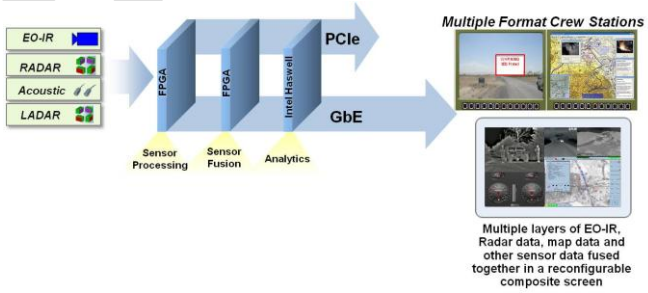

Figure 5: Integrated Sensor Fusion

CONCLUSION

The vehicle electronics architecture under development at General Dynamics Land Systems provides for rapid integration of emerging high bandwidth sensor applications. The electronic architecture is optimized for large data flows and real time processing that enables future growth including integration of advanced sensor technology providing our warfighters with the advantages of situational understanding and active protection systems. The low latency data and protocol conversion technology provide the means to integrate both new and legacy components that are compliant to VICTORY architecture standards and interface specifications. Modernization and incremental updates can be easily and affordably managed well into the future without any major infrastructure changes.