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3 UNIT (3U) OPENVPX RADIO CARD MODULE DEVELOPMENT FOR HARDWARE/SOFTWARE CONVERGENCE PROGRAM

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ABSTRACT

This paper will present a 3 Unit (3U) OpenVPX™ form factor radio card module technology for a 3U OpenVPX™ form factor chassis which supports Phase 1 of the U.S. Army Communications-Electronics Research, Development and Engineering Center's (CERDEC's) Hardware/Software Convergence (HWC) Program.

INTRODUCTION

The Space and Terrestrial Communications Directorate (S&TCD) developed a 3 Unit (3U) OpenVPX™ form factor radio card module for a 3U OpenVPX™ form factor chassis in support of Phase 1 of U.S. Army Communications-Electronics Research, Development and Engineering Center's (CERDEC's) Hardware/Software Convergence (HWC) Program. The goal of the program is to develop and execute a plan to achieve a modular, open family of hardware and software components for implementing interoperable Command, Control, Communications, Computers, Intelligence, Surveillance, and Electronic Warfare (C4ISR/EW) capabilities on Army ground platforms and enhance existence within the Size, Weight and Power and Cost (SWaP-C) constraints of these platforms. During Phase 1 of the HWC program, S&TCD partnered with BAE Systems Information and Electronic Systems Integration, Wayne, NJ design team in developing a 3U OpenVPX™ form factor radio card module which allowed unclassified communications with Army program of record (POR) radio systems. In addition to demonstrating support for a 3U OpenVPX™ form factor modular cards and chassis, other open families of hardware and software architectures and specifications supported by this effort include the Vehicular Integration for C4ISR/EW Interoperability (VICTORY) and Modular Open Radio Frequency Architecture (MORA). Figure 1 depicts the Major Components of the HW/SW Convergence Program:

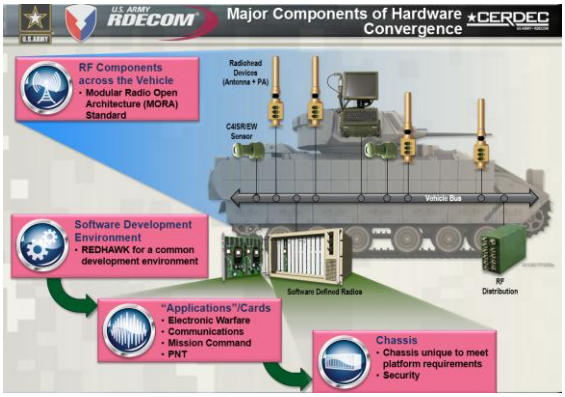

Figure 1: Major Components of the HWC Program [1]

HWC Program Goals, Standards and Specifications

The goals for current Phase 1 of HWC Program are listed below [2]:

- Demonstrate potential for improved SWaP via a common chassis for C4ISR/EW.
- Define an architecture at the hardware, software, and network layers.
- Validate the architecture by integrating Electronic Warfare (EW), Communications, Position, Navigation and Timing (PNT), and Sensors.
- Develop standards for Radio Frequency (RF) distribution.
- Select a high speed bus for real-time coordination.
- Research and select a backplane.
- Investigate Information Assurance (IA) and Electromagnetic Interference (EMI) concerns with a common chassis.
- Tabletop Technology Readiness Level (TRL) 4 Demonstration.

These efforts above will develop and mature standards and specifications for a converged architecture by the end of Phase 3. The ultimate goal is to transition the resulting standards and specifications to the acquisition community for inclusion in future solicitations and requirements [2].

For the Phase 1 TRL 4 (lab/bench-top) demonstration, S&TCD's 3U OpenVPX™ radio card module was integrated and simultaneously operated in a developmental 3U OpenVPX™ chassis with 3U OpenVPX™ cards from the following CERDEC organizations; the Intelligence and Information Warfare Directorate (I2WD) for EW and Radio Frequency Distribution Device (RFDD), the Command, Power and Integration Directorate (CPID) for PNT and Mission Command, and the Night Vision and Electronic Sensors Directorate (NVESD) for Multi-Functional Display (MVD), Camera and Sensor. Additionally, there was operation with an external (to the chassis) MVD device (from NVESD) and RadioHead (from I2WD) devices that demonstrated VICTORY and MORA support. For Phases 2 and 3, the HWC program will mature all these technologies to support a TRL 7 (prototype system in an operational environment) in a ruggedized 3U OpenVPX™ chassis with 3U OpenVPX™ cards, MVD and RadioHead. S&TCD's 3U OpenVPX™ radio card module may be modified in future Phases to support additional waveforms/capabilities to demonstrate multi-functional Software Defined Radio (SDR) operation.

3U OpenVPX™ Radio Card Module Development

The 3U OpenVPX™ radio card module development leverages a mature (TRL 6+) Core Engine transceiver design capable of operating in the Ultra High Frequency (UHF) and L-Band. This transceiver, developed by BAE Systems, is repackaged into a 3U conduction cooled OpenVPX™ module with dimensions length = 6.75" (160mm), height = 3.95" (100mm) and width (pitch) = 1". This module card is depicted in Figure 2 below:

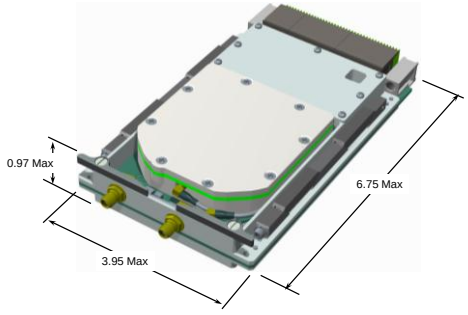

Figure 2: 3U Open VPX™ Radio Card Module

Radio Card Module Software

For Phase 1, the radio card module provided software components to support multiple tactical radio communications modes. Software for the 3U OpenVPX™ radio card module is ported from the Joint Tactical Networking Center (JTNC) DoD Waveform Information Repository. The Operating Environment (OE) and Waveform Software is maintained in this repository including source code and documentation for vendors to use who obtain proper permissions from the JTNC. BAE Systems 3U OpenVPX™ radio card module had this software installed on it, which allowed support of multiple tactical radio communications capabilities.

Phase 1 HWC Program 3U OpenVPX™ Chassis Profiles

In the development the 3U OpenVPX™ radio card module, the S&TCD and BAE Systems team participated in CERDEC's C4ISR/EW Hardware/Software Convergence Working-Level Integrated Product Team Program (HWC-WIPT) which included S&TCD, I2WD, CPID and NVESD from CERDEC, the MITRE Corporation and other private industry membership. One of the first major tasks for the HWC-WIPT was to develop the 3U OpenVPX™ Chassis profiles (definitions which follows) for the HWC program:

Backplane Profile - A physical definition of a backplane implementation that includes details such as the number and type of slots that are implemented and the topologies used to interconnect them. This profile is a description of Channels and Buses that interconnect slots and other physical entities in a backplane. For Phase 1, the HWC-WIPT defined a 12 slot backplane using 3U OpenVPX™ backplane profile BKP3-CEN12-15.2.6-3 from VMEbus™ International Trade Association (VITA) 65 [3].

Slot Profile - A physical mapping of Ports onto a given slot's backplane connectors. These definitions are often made in terms of Pipes. Slot Profiles also give the mapping of Ports onto Plug-In Module's backplane connectors. Unlike Module Profiles, a Slot Profile never specifies protocols for any of the defined Ports. For Phase 1, the HWC-WIPT used the 3U OpenVPX™ payload slot profile SLT3-PAY-1F2F2U-14.2.2 from VITA 65 [3]. For the Phase 1 HWC Demonstration, only the control plane was used; the data plane and expansion plane was not used but may be used in future Phases of the HWC program.

Module Profile - A physical mapping of Ports onto a given Module's backplane Connectors and protocol mapping(s), as appropriate, to the assigned Port(s). This definition provides a first-order check of operating compatibility between Modules and slots as well as between multiple Modules in a Chassis. Module profiles support slot profiles. For Phase 1, the HWC-WIPT used the 3U OpenVPX™ payload module profile MOD3-PAY-1F2F2U-16.2.2-4 14.2.2 from VITA 65 [3].

Figure 3 depicts the interconnections between the 3U OpenVPX™ radio card module and the chassis.

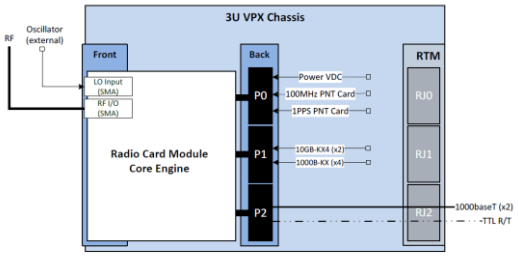

Figure 3: 3U Open VPX™ Radio Card Module in 3U VPX Chassis

Phase 1 included 1000BASE-KX over the control plane as well as a Transmit/Receive (T/R) discrete signal to communicate with the Radiohead hardware. A 10GbE data plane was also developed for future growth to support high speed MORA commands to the radio card module. The 3U OpenVPX™ radio card module accepts 3.3V, 5V, and 12V from the chassis power supply over the utility plane. Additionally, the 3U OpenVPX™ radio card module accepts a 1 Pulse per Second (PPS) auxiliary clock and 100MHz reference clock from the 3U OpenVPX™ PNT card via the utility plane. The PNT card provides a stable clock reference and 1PPS that enable radio card module to instantiate and perform operations in a network.

The 3U OpenVPX™ radio card module was designed to implement these slot and module profiles. For Phase 2 and 3, the backplane, slot and profiles will be reviewed and modified after feedback from the acquisition community and private industry.

MORA and RadioHead Support

For the HWC program, MORA is the approach to defining open architectures, standards and specifications for next generation multifunction SDRs. Referring to Figure 1, a key MORA concept is the separation of signal processing from signal conditioning. Signal processing will be performed on cards within the 3U OpenVPX™ chassis. Signal conditioning will be implemented in a RadioHead device which is externally and/or remote mounted on a typical

military vehicle directly connected to an antenna to minimize losses due to cabling [2]. For the early Phases of the HWC program, the RadioHead will contain the final stage power amplification on the transmit side and the Low Noise Amplifier (LNA) on the receive side and the signal path connection between the 3U OpenVPX™ chassis and the RadioHead will be an analog signal via a RF cable. Future Phases of the HWC program will support "Digital RF Distribution". In this paradigm, the Digital to Analog Converter (DAC) function, the frequency up conversion function and all power amplification on the transmit side and the LNA, gain stages, the frequency down conversion function and Analog to Digital Converter (ADC) function on the receive side, as well as transmit/receive filtering, will all be implemented in the Radiohead. This will allow the connection between the chassis and the RadioHead to be a digital signal via Ethernet or Fiber Optic cable. The RadioHead will also implement the Transmit/Receive (T/R) switch function to the antenna. For Phase 1 of the HWC program, the T/R control signal between the chassis and RadioHead will be a low voltage (3.3V) Transistor/Transistor Level (TTL) level "discrete" signal. For Phase 2 and 3, this control signal will be implemented via a high speed, low latency Ethernet protocol via Ethernet cable. Key Benefits of the MORA/RadioHead concept are listed below [1-2]:

- Reduces RF cable losses on the transmit side which will allow lower transmit power (which minimizes peak and average Direct Current (DCP power draw) to be used for same range.
- Reduces RF cable losses on the receive side which will increase RF receive sensitivity (Integrated LNA).
- Cooler crew cabin for military vehicles as the main heat generating element of a military radio system (the transmit power amplification) is external to the cabin.
- Establishes pooled resources that can be dynamically configured to accommodate mission requirements or mitigate system failures.
- Reduces SWaP on military vehicles by sharing hardware such as amplifiers and antennas.
- Improves efficiency by routing low power RF signals between components.
- Establishes open message interfaces that support management operations and real-time coordination.
- Enables system-of-systems Command and Control (C2) and Situational Awareness (SA) using a common display.

The 3U OpenVPX™ radio card module was configured to provide low output power to the RFDD for Phase 1 activities. The RF output of the module itself can be configured for higher power if necessary for future phases.

The 3U OpenVPX™ radio card module supports T/R discrete TTL level signaling (for Phase 1) required by the Radiohead for transmit/receive switching to a Power Amplifier. A high speed MORA interface capable of low latency Ethernet protocol via Ethernet cable (i.e., messages over 10GbE expansion plane) is also ready to be used as well for future Phases.

VICTORY, MORA, MVD and Radio Control/Status

For the HWC program, control and status can be accomplished/displayed on the touch-screen MVD device for all major components in Figure 1 in using the VICTORY Data Bus (VDB) and the MORA control/status interface. The VDB is the core mechanism for integration on the platform and is based on Ethernet IP which is the "convergence layer" between hardware and software components [2].

Control, status and command of the 3U OpenVPX™ radio card module is provided by a set of Modular Open RF Architecture (MORA) commands developed as part of the Phase 1 Hardware Convergence program. These MORA commands implement a standard set of Software Defined Radio (SDR) Management interface (ie web service) messages. These messages implemented functions to facilitate the Human Machine Interface (HMI) and allow a Mission Vehicle Display (MVD) to control/status and command the radio card module to

- Select / Change presets commands,
- Adjust volume,
- Call Groups,
- Inhibit transmit functions
- Send status (system health) information to MVD

Status polling for Phase 1 occurred every 10 seconds to the MVD including a SysLog command that provided health status of the radio card module. Additional MORA interface definition continue in Phase 2 and 3 to allow full control and status of the radio card module including: authentication, instantiation, network statistics, key management, and power on/off.

Radio Card Testing Phase 1 Throughput Testing

The 3U OpenVPX™ radio card module demonstrated UHF and L-Band voice and data communication during Phase 1.

Point-to-Point testing, including data verification, was demonstrated as expected based on the tactical radio mission plans (developed with help from the MITRE Corporation) implemented. Point-to-Point testing was done with multiple POR tactical radio systems.

Phase 1 Tabletop (TRL 4) Demonstration

A Phase 1 tabletop (TRL 4) HWC Demonstration was for key stakeholders in the R&D and acquisition community. The following was successfully demonstrated:

- Voice communication from a push to talk headset using a H250 Handset Interface.
- UHF and L-Band voice and data communication.
- Interoperability with POR tactical radio systems for voice and data.
- Control and Status of the 3U OpenVPX™ radio card module via the MVD using a common MORA interface.
- Sharing of common RF comments (RFDD and Radioheads).
- The radio card module serving as a the data transport service for a Command and Control (C2) link, which allowed Situational Awareness (SA) information to be controlled and displayed via the MVD.
- Simultaneous operation in a developmental 3U OpenVPX™ chassis with other 3U OpenVPX™ module cards, to include the module card from I2WD executing a simulated EW scenario and the module card from NVESD showing real time Camera and Sensor imagery via the MVD while all module cards shared common timing sources via the PNT card from CPID. This was key Phase 1 demonstration objective for the HWC program.

Conclusion

The 3U OpenVPX™ radio card module developmental effort detailed in this paper demonstrated support and initial verification of the slot and chassis profiles for 3U OpenVPX™ form factor modular cards and chassis, and other open families of hardware and software architectures and specifications such as the Vehicular Integration for C4ISR/EW Interoperability (VICTORY) and Modular Open Radio Frequency Architecture (MORA). A Phase 1 Tabletop (TRL 4) Demonstration successfully achieved a critical Phase 1 milestone of simultaneous operation of multiple HWC Program technologies in the same developmental 3U OpenVPX™ chassis. The HWC Program will proceed to Phase 2 of the development effort and will incorporate feedback and design considerations developed during this Phase 1 effort to advance the program.

REFERENCES

[1] P. Zablocky, “Hardware Convergence, A Game Changing Approach for the Future”, Technology Day Presentation for Industry, April 2015

[2] B. Peddicord, “CERDEC C4ISR/EW Hardware/Software Convergence”, Technology Day Presentation for Industry, April 2015

[3] American National Standards Institute Inc., “ANSI/VITA 65-2010 (R2012) OpenVPX™ System Specification”, February 2012